RF Electro-Thermal Modeling of LDMOSFETs for Power-Amplifier Design

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***Abstract*—A new approach for the electro-thermal modeling of LDMOSFETs for power-amplifier design that bypasses pulsed-*IV*s and pulsed-RF measurements is presented in this paper. The existence of low-frequency dispersion in LDMOSFETs is demonstrated by comparing pulsed IVs with iso-thermal *IV*s. The modeling technique uses iso-thermal *IV* and microwave measurements to obtain the temperature dependence of small-signal parameters. Optimized tensor-product B-splines, which distribute knots to minimize fitting errors, are used to represent the small-signal parameters and extract the large-signal model as a function of voltages and temperature. The model is implemented on ADS and is verified by simulating and measuring the power harmonics and IMD large-signal performance of a power amplifier. The impact on the model of temperature-dependent drain and gate charge is investigated. The presented model is found to compare well and, in some cases, exceed the existing MET model for LDMOSFETs.**

***Index Terms*—B-spline representation, electrothermal FET model, LDMOSFET, nonquasi-static equivalent circuit, RF power amplifiers.**

I. Introduction

PACKAGED silicon power LDMOSFETs are finding increasing use for linear RF power amplification. Such devices are now unseating traditional heterojunction bipolar transistors (HBTs) and high electron-mobility transistors (HEMTs) at frequencies up to 2.3 GHz for cellular base stations and high-power transmitters [1], [2]. The increasing use of these devices calls for better models targeted toward RF power-amplifier design [3]. Collantes *et al.* [4] recently proposed a nonelectro-thermal pulsed-*IV* measurement-based table model using approximation B-splines. Pulsed *IV*s have been used extensively for modeling of devices that suffer from low-frequency dispersion, either due to thermal, trapping, or parasitic bipolar effects [5]. However, because of the fact that pulsed *IV*s depend upon the original bias point used to generate them, there are an infinite number of different pulsed-*IV*s characteristics possible. B-splines and their tensor representation have also been used extensively in modeling of FETs [6]–[8].

Motorola's electro-thermal model (MET) [9], a variant of the Curtice model [10], uses cold-biased pulsed *IV*s and corresponding pulsed-RF measurements to extract a full electro-thermal model of the LDMOSFET. However, most microwave laboratories unfortunately do not possess such expensive equipment and, hence, need to use other approaches to acquire iso-thermal data for extracting device models for power devices.

This paper presents an alternative approach that uses iso-thermal *IV*s and microwave measurements to extract a full electro-thermal model of LDMOSFETs. It begins by explaining the iso-thermal *IV* measurement technique and comparing iso-thermal *IV*s with pulsed *IV*s. The temperature dependence of small-signals parameters is demonstrated. Three-dimensional (3-D) tensor product B-splines (TPSs) are used to represent small-signal parameters as a function of drain–source and gate–source voltages and average device temperature, and are used to extract large-signal parameters. The developed model is implemented in the ADS circuit simulator and used for power-amplifier simulations. Performance matrices predicted in ADS, such as power harmonics and intermodulation distortion (IMD), are compared with measured results to verify the modeling approach.

II. DC, Iso-Thermal, and Pulsed *IV*s

For this entire study, we have used Motorola's MRF 181 RF power n-channel-enhancement-mode lateral diffused MOSFET [11]. The MRF 181 has a total gatewidth of 20.16 mm, a gate length of 1.5 μm, and a maximum junction to case thermal resistance of 5.42 °C/W.

A normal dc current–voltage–temperature (IVT) of a device is measured by setting the substrate temperature $(T_{\rm sub})$ and gate–source and drain–source voltages $(V_{\rm GS}, V_{\rm DS})$ and by measuring the drain current $(I_{\rm DS})$ and the average surface device temperature $(T_{\rm dev})$ using an infrared thermometer. Fig. 1 shows the measured dc IVT for a $T_{\rm Sub}$ of 35 °C and a $V_{\rm GS}$ range from 4 to 6.5 V in steps of 0.25 V. The device temperature is superimposed on the curve. Using a least-squares fit on the measured device-temperature versus intrinsic-device power characteristics for all bias points (see Fig. 2), we can extract the thermal resistance $R_{\rm th}$ in the electro-thermal model proposed in Fig. 3 [12].

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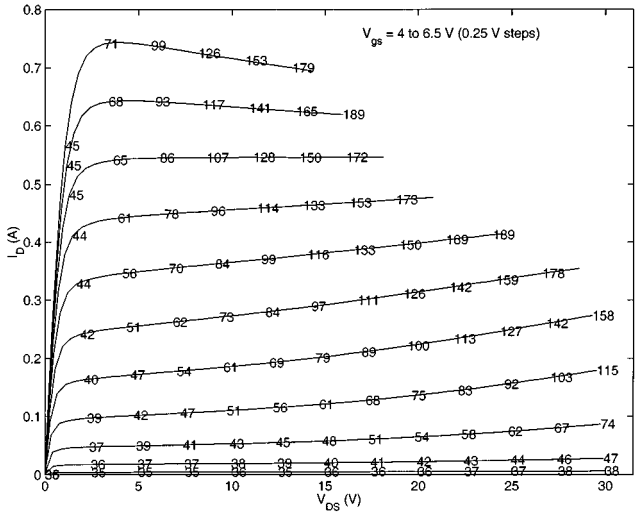

Fig. 1. Measured *IV*, with $T_{\rm dev}$ superimposed, for a constant substrate temperature of 35 °C.

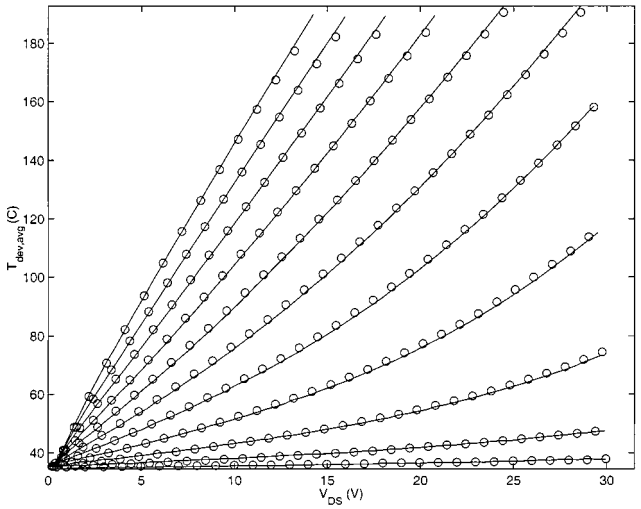

Fig. 2. Prediction of device temperature (solid lines) compared with measured values (circles) using a single $R_{\rm th}$ for a given $T_{\rm sub}$ of 35 °C.

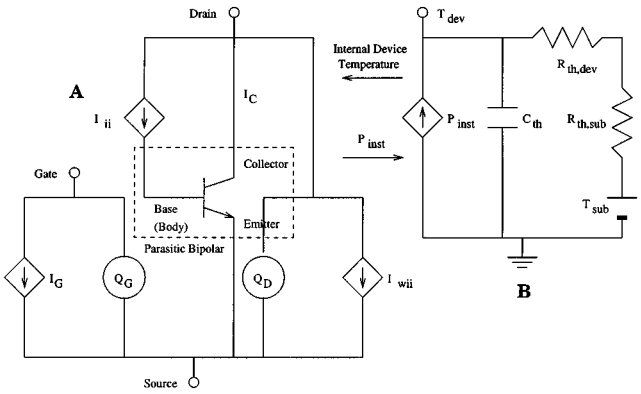

Fig. 3. (A) Intrinsic self-biasing model topology to fit both dc and RF. (B) Electrical network representing the thermal network model for the thermal boundary conditions used.

Using this $R_{\rm th}$ value, the device temperature for a given bias can then be computed. The solid lines in Fig. 2 show the predicted $T_{\rm dev}$ for a $T_{\rm sub}$ of 35 °C, while the circles give the measured $T_{\rm dev}$. A single $R_{\rm th}$ value does an excellent job in mapping the entire device average thermal response at dc.

The curves given in Fig. 1 yield on differentiation the effective dc conductance $(g_{d,\rm dc})$ and transconductance $(g_{m,\rm DC})$, which will differ from the ac conductance $(g_{d,\rm RF})$ and transconductance $(g_{m,\rm RF})$ due to low-frequency dispersion effects. Such dispersion can be caused by either thermal and/or parasitic effects. While III–V and silicon on insulator (SOI) devices suffer from both these effects, it is generally thought that thermal effects are the major contributor to low-frequency dispersion in LDMOSFETs. The p+ sinker diffusion kills the floating base bipolar and, hence, dispersion from this and similar mechanisms are not expected.

An approach to verify this would be to measure *IV*s that isolate the two major contributors to dispersion. Pulsed *IV* measurements are iso-thermal in nature, bypassing both of these dispersion effects and can be used as one measure. On the other hand, a measurement scheme that bypasses only thermal effects will yield a true iso-thermal *IV*.

A novel approach to directly measure iso-thermal *IV*s has been implemented under computer control [13]. In this approach, the substrate is set to the lowest temperature (in this case, cooled to 18 °C) and $V_{\rm GS}$ is set to its highest value. $V_{\rm DS}$ is then swept and the drain current at all data points within ±2 °C of the targeted $T_{\rm dev}$ are recorded after establishing thermal equilibrium. $V_{\rm GS}$ is then lowered and the process continues. Once the data has been acquired for the lowest $V_{\rm GS}$, the substrate temperature is increased and the process is repeated.

In essence, the technique is an efficient algorithm used to vary the substrate temperature and efficiently search for all bias combinations giving a targeted constant $T_{\rm dev}$. The lower the substrate temperature, the higher the bias point that will give the targeted $T_{\rm dev}$. Hence, due to limitations on cooling the substrate, data cannot be acquired at high bias values. An *IV* measured with this technique is essentially iso-thermal while still retaining the effects of any low-frequency dispersion due to other than thermal effects.

Fig. 4 compares a 75 °C iso-thermal *IV* $I_{D,\rm iso}(V_{\rm GS}, V_{\rm DS}, T_{\rm dev})$ (solid lines) with a pulsed *IV* $I_{D,\rm puls}(v_{\rm GS}, v_{\rm DS}, 0, 0, T_{\rm dev} = T_{\rm sub})$ generated by setting $T_{\rm sub}$ at 75 °C for a cold-biased (zero dc bias) device (dashed line) and a pulsed *IV* $I_{D,\rm puls}(v_{\rm GS}, v_{\rm DS}, V_{\rm GS}, V_{\rm DS}, T_{\rm dev})$ generated from a hot-biased $(V_{\rm GS}, V_{\rm DS})$ device (dashed–dotted lines) yielding a $T_{\rm dev}$ of 75 °C. The star indicates the bias point used for the hot-biased pulsed *IV*s, which are measured for a $T_{\rm sub}$ of 45 °C. Fig. 5 shows a similar curve at a $T_{\rm dev}$ of 105 °C. For a meaningful comparison of the iso-thermal and pulsed *IV*s, the cold- and hot-biased pulsed *IV* curves were shifted down by 10 mA to account for a difference in equipment calibration and enforce the required dc-bias condition that the hot-biased pulsed *IV* and isothermal *IV* curves intersect at the dc-bias point $(V_{\rm GS}, V_{\rm DS})$ as follows:

$$I_{D,\rm puls}(v_{\rm GS} = V_{\rm GS}, v_{\rm DS} = V_{\rm DS}, V_{\rm GS}, V_{\rm DS}, T_{\rm dev}) = I_{D,\rm iso}(V_{\rm GS}, V_{\rm DS}, T_{\rm dev}). \quad (1)$$

From Figs. 4 and 5, it can be observed that the iso-thermal *IV*s are in good agreement with the hot-biased pulsed *IV*s. For 75 °C, the hot- and cold-biased pulsed *IV*s are in agreement at mid drain currents (0.2 A), but can depart significantly at high

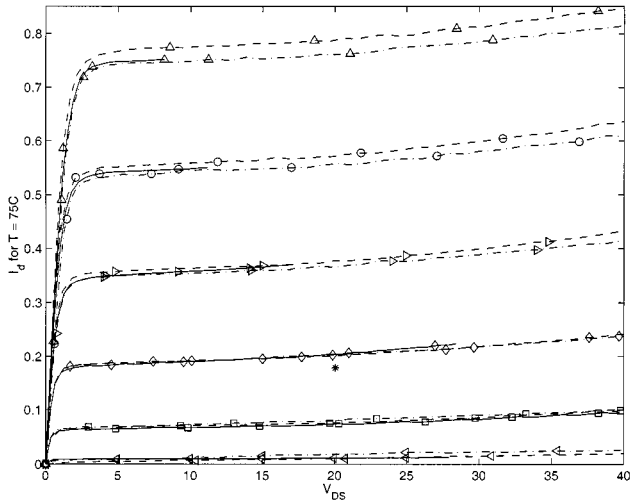

Fig. 4. Comparison between iso-thermal *IV* (solid lines), cold pulsed *IV*s (dashed lines), and hot-biased pulsed *IV*s (dashed–dotted line) for $T_{\rm dev}$ of 75 °C. * denotes the bias point used for hot-biased pulsed *IV*s. $V_{\rm GS}$ ranges from 4 to 6.5 V in steps of 0.5 V. ◁ denotes $V_{\rm GS} = 4$ V, □ denotes $V_{\rm GS} = 4.5$ V, ◇ denotes $V_{\rm GS} = 5$ V, ▷ denotes $V_{\rm GS} = 5.5$ V, ○ denotes $V_{\rm GS} = 5.5$ V, and △ denotes $V_{\rm GS} = 6$ V.

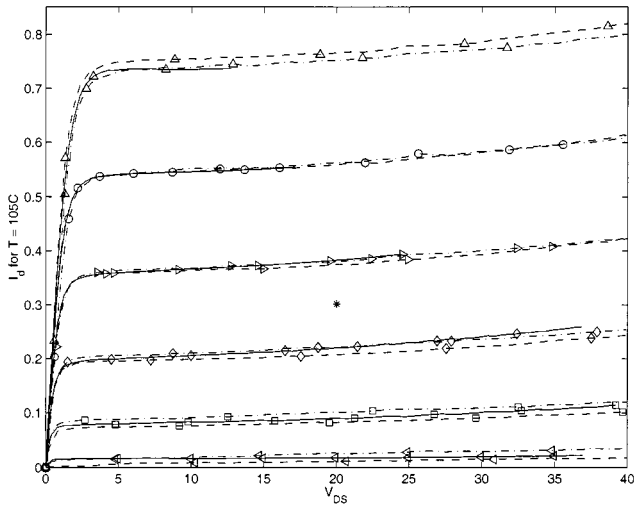

Fig. 5. Comparison between iso-thermal *IV* (solid lines), cold pulsed *IV* (dashed lines) and hot-biased pulsed IV (dashed–dotted line) for $T_{\rm dev}$ of 105 °C. * denotes the bias point used for hot-biased pulsed *IV*s. $V_{\rm GS}$ ranges from 4 to 6.5 V in steps of 0.5 V. ◁ denotes $V_{\rm GS} = 4$ V, □ denotes $V_{\rm GS} = 4.5$ V, ◇ denotes $V_{\rm GS} = 5$ V, ▷ denotes $V_{\rm GS} = 5.5$ V, ○ denotes $V_{\rm GS} = 5.5$ V, and △ denotes $V_{\rm GS} = 6$ V.

and somewhat at low currents. This trend is also observed for similar measurements at higher and lower temperatures. However, for similar curves measured at 45 °C, the hot- and cold-biased pulsed *IV*s were found to agree well.

It is safe to conclude that the LDMOSFET does indeed suffer from some dispersion effects, which clearly become more profound at higher device temperatures (corresponding to biasing the device at higher drain currents). This dispersion, however, is not as profound as that suffered by III–V devices or floating-body SOI devices, due to the presence of the p+ sinker body tie in LDMOSFETs.

Given the fact that there can be much variation among cold- and hot-biased pulsed *IV*s, which are functions of their starting bias point, and that for a wide range of temperature, the iso-thermal *IV*s agree well with the hot-biased pulsed *IV*s, the iso-thermal *IV*s can be used as an alternative data source to pulsed *IV*s.

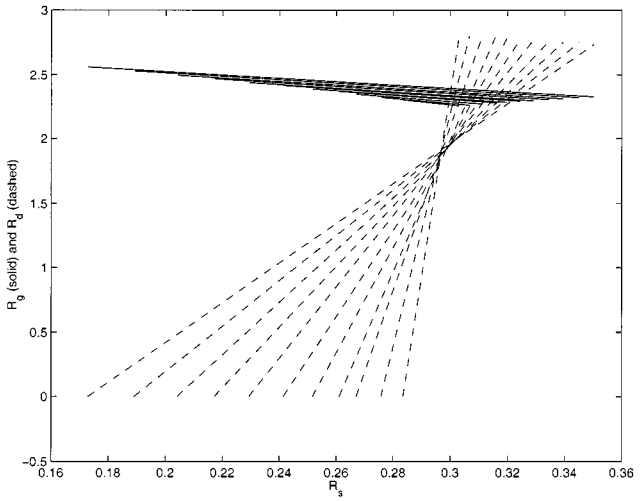

Fig. 6. Trajectories of R_g (solid lines) and R_d (dashed lines) as a function of R_s for a constant $I_{\rm DS}$.

III. Temperature-Dependent Small-Signal Parameters

The iso-thermal *IV* measurement tool can also be used to acquire iso-thermal S-parameters. By using this scheme, iso-thermal microwave data was acquired at temperatures ranging from 45 °C to 105 °C in steps of 15 °C. A thru-reflect line (TRL) was used to obtain calibrated data at the gate and drain planes.

The Y-parameters of the intrinsic small-signal topology [18], [12] can be written as $Y_{ij} = g_{ij} + j\omega C_{ij}/(1 + j\omega\tau_{ij})$, where C_{ij}, g_{ij}, and τ_{ij} are the bias-dependent capacitance (transcapacitance), conductance (transconductance), and nonquasi-static (NQS) times constants, respectively. Note that $g_{11} = g_{12} = 0$, $g_{21} = g_m$, and $g_{22} = g_d$. A two τ approximation can be made such that $\tau_{11} = \tau_{12} = \tau_G$ and $\tau_{21} = \tau_{22} = \tau_D$.

The microwave data is deembedded using the NQS multibias approach given in [14] and [15] to extract small-signal parameters and device parasitics. This involves fitting the extrinsic Z-parameters and then using analytical expressions for intrinsic and extrinsic parameters that are functions of Z-parameter fitting constants. These expressions indicate a continuum of solutions as a function of R_s, the source parasitic resistance. A multibias analysis is used to plot the R_d and R_g trajectories as a function of R_s for different bias points for the same drain current as shown in Fig. 6. The intersection point gives the R_s value. The bias resistances are found to increase slightly with increasing drain current. Due to the relatively small values of the parasitics, their possible temperature dependence has been neglected.

Fig. 7 shows that the resulting S-parameter fits at $V_{\rm GS} = 5.5$ V and $V_{\rm DS} = 15$ V and $T_{\rm dev}$ of 90 °C. The small-signal model does an excellent job in fitting the device microwave parameters.

Figs. 8 and 9 show the variation in the raw extracted g_m and g_d as a function of device temperature over all measured bias points. Note that the extrinsic $V_{\rm DS}$ values plotted are a bit

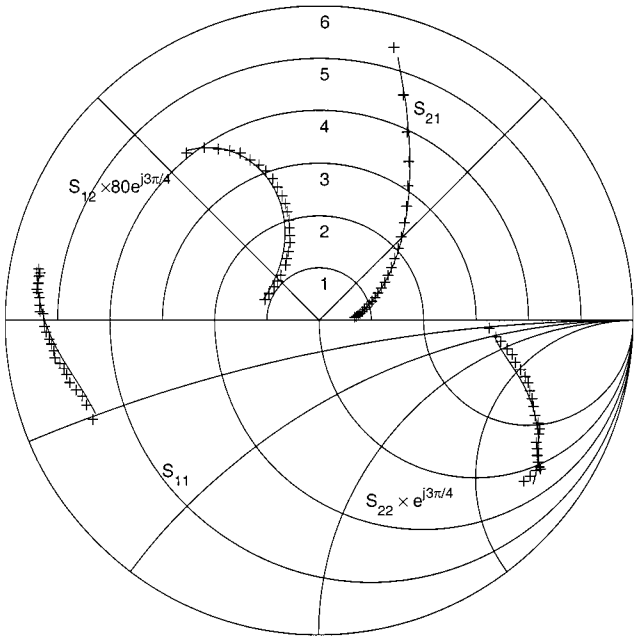

Fig. 7. Comparison between fitted S-parameters (solid lines) and measured data (plus signs) for $V_{\rm GS} = 5.5$ V, $V_{\rm DS} = 15$ V, and $T_{\rm dev}$ of 90 °C.

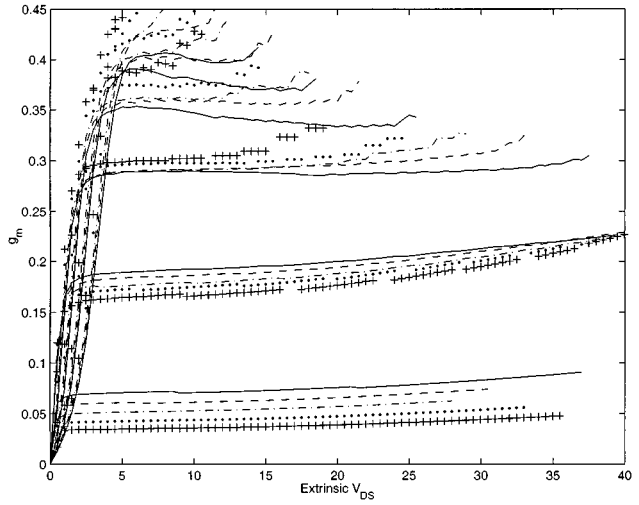

Fig. 8. Extracted g_m for $V_{\rm GS} = 4$ V to 6.5 V in steps of 0.5 V for different $T_{\rm dev}$: $T_{\rm dev} = 105$ °C (solid lines), $T_{\rm dev} = 90$ °C (dashed lines), $T_{\rm dev} = 75$ °C (dashed–dotted lines), $T_{\rm dev} = 60$ °C (dotted lines), and $T_{\rm dev} = 45$ °C (plus signs).

skewed as a result of the parasitic present in the dc-biasing network. $V_{\rm GS}$ is from 4 to 6.5 V in steps of 0.5 V. Solid lines are for a $T_{\rm dev}$ of 105 °C, dashed lines are a $T_{\rm dev}$ of 90 °C, dashed–dotted lines are for a $T_{\rm dev}$ of 75 °C, dotted lines are for a $T_{\rm dev}$ of 60 °C, and plus signs are for a $T_{\rm dev}$ of 45 °C, respectively.

It can be seen from Figs. 8 and 9 that while g_d is relatively temperature independent, g_m is quite sensitive to temperature.

Figs. 10–13 show the variation in the raw extracted C_{11}, C_{12}, C_{21}, and C_{22} as a function of device temperature over all measured bias points. The plot line styles used to denote different temperature values before have been used for these parameters. The $V_{\rm DS}$ and $V_{\rm GS}$ ranges are also as before.

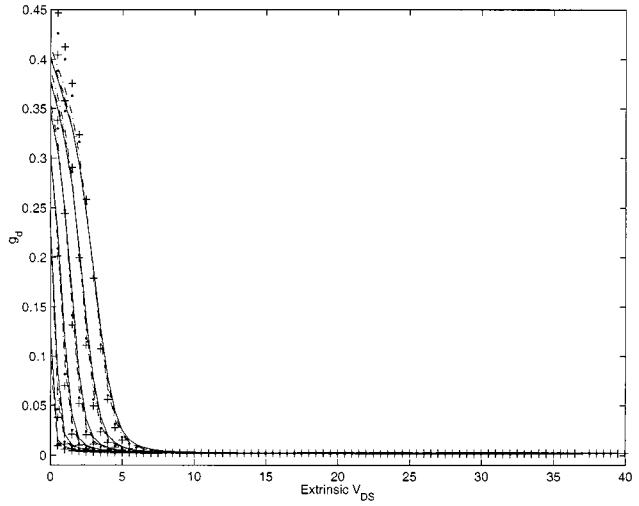

Fig. 9. Extracted g_d for $V_{\rm GS} = 4$ V to 6.5 V in steps of 0.5 V for different $T_{\rm dev}$: $T_{\rm dev} = 105$ °C (solid lines), $T_{\rm dev} = 90$ °C (dashed lines), $T_{\rm dev} = 75$ °C (dashed–dotted lines), $T_{\rm dev} = 60$ °C (dotted lines), and $T_{\rm dev} = 45$ °C (plus signs).

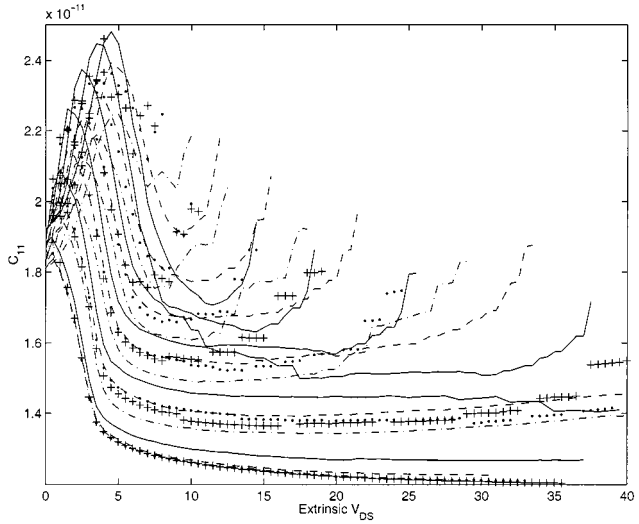

Fig. 10. Extracted C_{11} for $V_{\rm GS} = 4$ V to 6.5 V in steps of 0.5 V for different $T_{\rm dev}$: $T_{\rm dev} = 105$ °C (solid lines), $T_{\rm dev} = 90$ °C (dashed lines), $T_{\rm dev} = 75$ °C (dashed–dotted lines), $T_{\rm dev} = 60$ °C (dotted lines), and $T_{\rm dev} = 45$ °C (plus signs).

It can be seen in Figs. 10–13 that while C_{12} and C_{22} are relatively temperature independent, C_{11} and C_{21} are temperature dependent. This fact can be used to simply the charge extraction.

Due to the cooling limitation of the substrate temperature controller used, microwave small-signal data is unavailable at high gate and drain voltages. Ideally, a pulsed dc and pulsed RF technique can be used to access this region without cooling the substrate. However, in the absence of such pulsed RF equipment for high-power transistors, an extrapolation scheme has been used to obtain data in this region.

IV. Large-Signal Modeling

The large-signal electro-thermal model for the LDMOSFET shown in Fig. 3 features a simple thermal network topology,

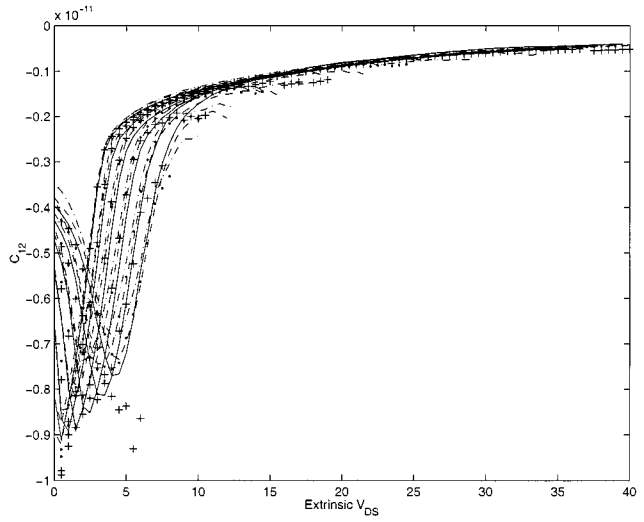

Fig. 11. Extracted C_{12} for $V_{\rm GS} = 4$ V to 6.5 V in steps of 0.5 V for different $T_{\rm dev}$: $T_{\rm dev} = 105\,^{\circ}$C (solid lines), $T_{\rm dev} = 90\,^{\circ}$C (dashed lines), $T_{\rm dev} = 75\,^{\circ}$C (dashed–dotted lines), $T_{\rm dev} = 60\,^{\circ}$C (dotted lines), and $T_{\rm dev} = 45\,^{\circ}$C (plus signs).

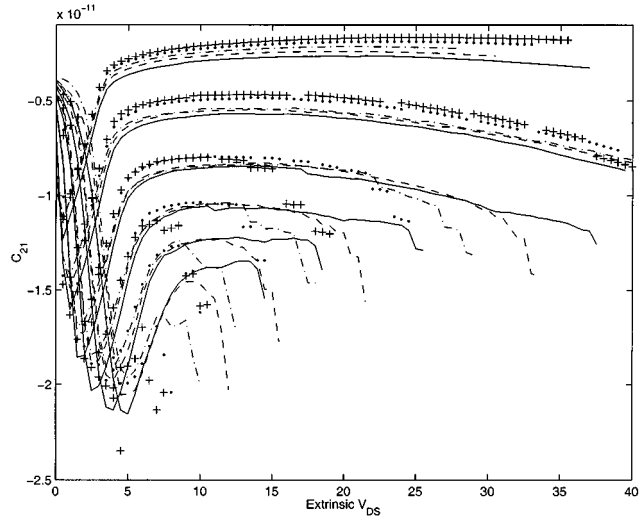

Fig. 12. Extracted C_{21} for $V_{\rm GS} = 4$ V to 6.5 V in steps of 0.5 V for different $T_{\rm dev}$: $T_{\rm dev} = 105\,^{\circ}$C (solid lines), $T_{\rm dev} = 90\,^{\circ}$C (dashed lines), $T_{\rm dev} = 75\,^{\circ}$C (dashed–dotted lines), $T_{\rm dev} = 60\,^{\circ}$C (dotted lines), and $T_{\rm dev} = 45\,^{\circ}$C (plus signs).

which calculates the steady state iso-thermal temperature of the LDMOSFET as a function of the power dissipated by the LDMOSFET. The model includes a parasitic bipolar driven by the impact ionization current so as to model low-frequency dispersion [12]. The large-signal representations can be obtained from the extracted small-signal model parameters using path-independent integration performed in this paper with tensor-product B-splines (one possible integration path is shown for the sake of clarity) as follows:

$$\begin{aligned} &I_{D,\rm puls}(v_{\rm GS}, v_{\rm DS}, V_{\rm GS}, V_{\rm DS}, T_{\rm dev}) \\ &\quad = \int_{V_{\rm GS}}^{v_{\rm GS}} g_m(V'_{\rm GS}, V_{\rm DS}, T_{\rm dev})\, dV'_{\rm GS} \\ &\qquad + \int_{V_{\rm DS}}^{v_{\rm DS}} g_d(v_{\rm GS}, V'_{\rm DS}, T_{\rm dev}) dV'_{\rm DS} \end{aligned}$$

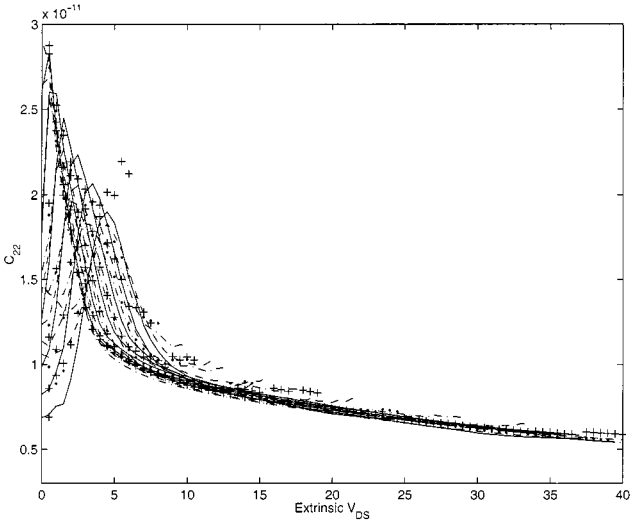

Fig. 13. Extracted C_{22} for $V_{\rm GS} = 4$ V to 6.5 V in steps of 0.5 V for different $T_{\rm dev}$: $T_{\rm dev} = 105\,^{\circ}$C (solid lines), $T_{\rm dev} = 90\,^{\circ}$C (dashed lines), $T_{\rm dev} = 75\,^{\circ}$C (dashed–dotted lines), $T_{\rm dev} = 60\,^{\circ}$C (dotted lines), and $T_{\rm dev} = 45\,^{\circ}$C (plus signs).

with

$$\begin{aligned} &I_{D,\rm puls}(V_{\rm GS}, V_{\rm DS}, V_{\rm GS}, V_{\rm DS}, T_{\rm dev}) \\ &\quad \simeq I_{D,\rm iso}(V_{\rm GS}, V_{\rm DS}, T_{\rm dev}) \\ &Q_G(v_{\rm GS}, v_{\rm DS}, V_{\rm GS}, V_{\rm DS}, T_{\rm dev}) \\ &\quad = \int_{V_{\rm GS}}^{v_{\rm GS}} C_{11}(V'_{\rm GS}, V_{\rm DS}, T_{\rm dev})\, dV'_{\rm GS} \\ &\qquad + \int_{V_{\rm DS}}^{v_{\rm DS}} C_{12}(v_{\rm GS}, V'_{\rm DS}, T_{\rm dev})\, dV'_{\rm DS} \\ &Q_D(v_{\rm GS}, v_{\rm DS}, V_{\rm GS}, V_{\rm DS}, T_{\rm dev}) \\ &\quad = \int_{V_{\rm GS}}^{v_{\rm GS}} C_{21}(V'_{\rm GS}, V_{\rm DS}, T_{\rm dev})\, dV'_{\rm GS} \\ &\qquad + \int_{V_{\rm DS}}^{v_{\rm DS}} C_{22}(v_{\rm GS}, V_{\rm DS}, T_{\rm dev})\, dV'_{\rm DS} \end{aligned} \tag{2}$$

where $v_{\rm GS}$ and $v_{\rm DS}$ are the pulsed-*IV* voltages at which the pulsed-*IV* current and charges are predicted (see [12]) for a dc-bias point of $V_{\rm GS}$ and $V_{\rm DS}$. Note that following our discussion in Section II, the dc-bias dependence of the pulsed *IV* and charges can be neglected in the LDMOSFET.

The extracted small-signal parameters are fitted using a knot optimized 3-D TPSs technique [16]. In this optimized knot placement technique, an error function is computed to determine how close a fit it is to the original data. The knot placement is then readjusted so that the knot concentration in the higher error region is increased, while reducing the concentration in the lower error region. Note that the overall number of knots in a particular bias direction are kept the same. It is only the knot distribution that is changed. This technique is necessary in light of the steep knee in the intrinsic device drain current. Nonoptimized TPSs are unable to handle these regions and give rise to oscillatory behavior.

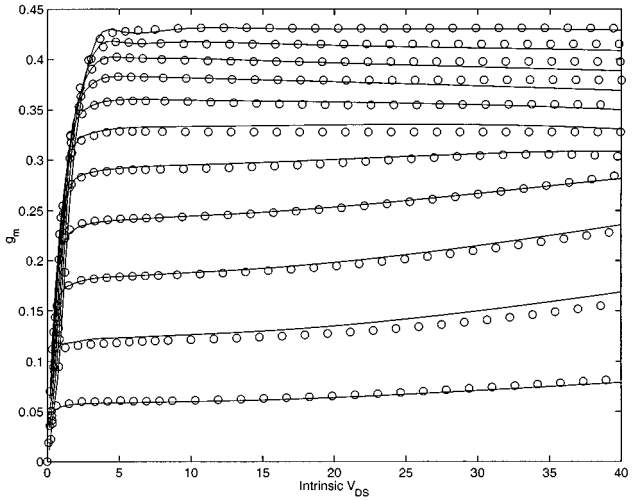

Fig. 14. Comparison of 3-D TPS fitted g_m (solid lines) with values extracted from the small-signal fit (circles) for $T_{\rm dev}$ of 90 °C. $V_{\rm GS}$ ranges from 4 to 6.5 V in steps of 0.25 V.

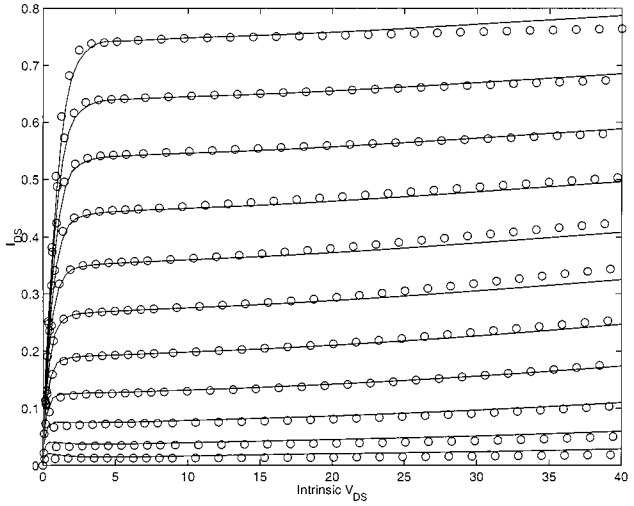

Fig. 15. Comparison of 3-D TPS fitted $I_{D,\rm iso}$ (solid lines) with measured values (circles) for $T_{\rm dev}$ of 90 °C. $V_{\rm GS}$ ranges from 4 to 6.5 V in steps of 0.25 V.

Using 3-D TPSs, a function of three variables can be represented as

$$S(V_{\rm GS},V_{\rm DS},T_{\rm DEV})=\sum_{i=1}^{m}\sum_{j=1}^{n}\sum_{l=1}^{p}a_{ijk}B_{i,k_{\rm GS},t_{\rm GS}}(V_{\rm GS})\times B_{j,k_{\rm DS},t_{\rm DS}}(V_{\rm DS})B_{l,k_{\rm DEV},t_{\rm DEV}}(T_{\rm DEV}) \tag{3}$$

where $k_{\rm GS},k_{\rm DS}$, and $k_{\rm DEV}$ are the B-spline orders in the $V_{\rm GS},V_{\rm DS}$, and $T_{\rm DEV}$ directions, respectively. $t_{\rm GS},t_{\rm DS}$, and $t_{\rm DEV}$ are the knot sequences in the $V_{\rm GS},V_{\rm DS}$, and $T_{\rm DEV}$ directions, respectively. $B_{i,k_{\rm GS},t_{\rm GS}},B_{j,k_{\rm DS},t_{\rm DS}}$, and $B_{l,k_{\rm DEV},t_{\rm DEV}}$ are one-dimensional B-spline polynomial functions, and a_{ijk} are the TPS coefficients that need to be determined.

Storage requirements for the TPS method are very reasonable since for $m=8,n=5$, and $p=4$, only 160 a_{ijk} coefficients are required. For $k_{\rm VG}=4,k_{\rm VD}=4$, and $k_{\rm DEV}=4$, only 64 coefficients are required to compute functional and derivative values at any particular bias point, due to the variation diminishing property of B-splines. Hence, computation proceeds rapidly. By using B-splines of order 4, second-order continuity is guaranteed. Also, mixed derivatives match, ensuring that the TPS method is naturally charge conserving [17].

A. Current

Using a 3-D knot optimized TPS, $g_{m,\rm RF}$ and $g_{d,\rm RF}$ are integrated and simultaneously fitted with the iso-thermal *IV* over all temperatures to obtain a 3-D representation of these functions. Figs. 14 and 15 show the fits of the intrinsic g_m and iso-thermal *IV* at a $T_{\rm dev}$ of 90 °C, respectively. The circles give the small-signal extracted and measured values (augmented by extrapolation in regions where data is unavailable), while the solid lines are the TPS representations. Fig. 16 shows the 3-D represented $g_{m,\rm RF}$ as a function of $T_{\rm dev}$ (solid lines). The circles are the extracted g_m for a $V_{\rm DS}$ of 10 V and a $V_{\rm GS}$ range from 4 to 6.5 V in steps of 0.25 V.

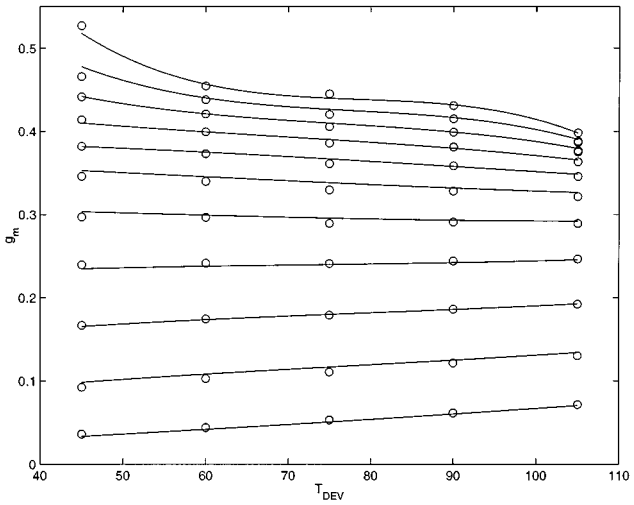

Fig. 16. Comparison of 3-D TPS fitted g_m (solid lines) with values extracted from the small-signal fit (circles) for $V_{\rm DS}=10$ V. $V_{\rm GS}$ ranges from 4 to 6.5 V in steps of 0.25 V.

B. Charge

In Figs. 10–13, it was observed that C_{12} and C_{22} are relatively temperature independent and C_{12} and C_{22} are temperature dependent. In order to simplify the large-signal model, the 60 °C C_{12} and C_{22} are used and the charge is made device temperature independent. This can be justified given the comparatively small temperature variation in capacitance, given their large values (in the order of 10^{-11} F). However, this will mean that, at higher RF power levels, where the average device temperature increases substantially, the accuracy of the model will begin to degrade. The effect of this simplification will be investigated later.

A further simplification is made to average out the NQS times such that 1 ps is used for the gate charge and 0.1 ps for the drain charge. Since the NQS times have most impact at frequencies approaching $f_{\rm max}$ [18], this has been verified to have a relatively small impact on the model and this approximation can easily be relaxed if needed.

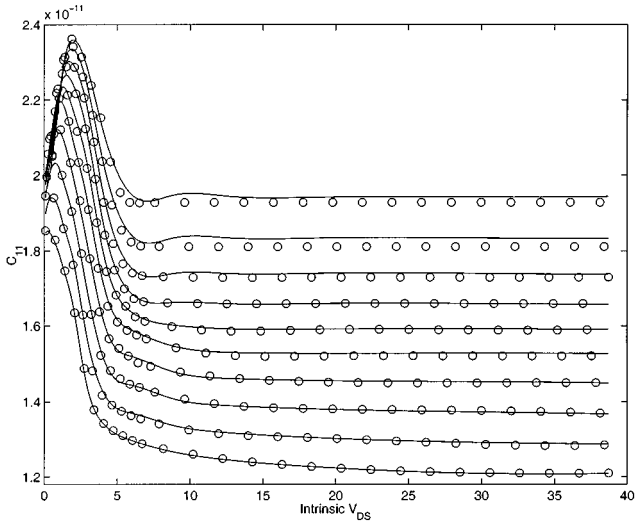

Fig. 17. Comparison of TPS fitted C_{11} at a $T_{\rm dev}$ of 60 °C (solid lines) with values extracted from the small-signal fit (circles). $V_{\rm GS}$ ranges from 4 to 6.25 V in steps of 0.25 V.

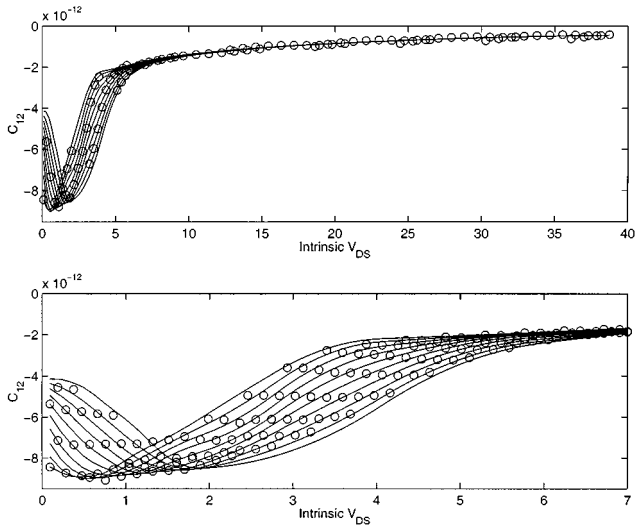

Fig. 18. Comparison of TPS fitted C_{12} at a $T_{\rm dev}$ of 60 °C (solid lines) with values extracted from the small-signal fit (circles). $V_{\rm GS}$ ranges from 4 to 6.25 V in steps of 0.25 V. The lower figure is a zoom on the upper figure.

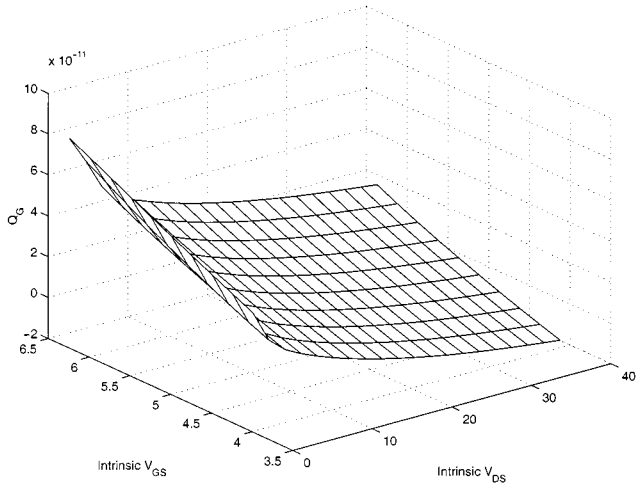

Fig. 19. TPS extracted gate charge.

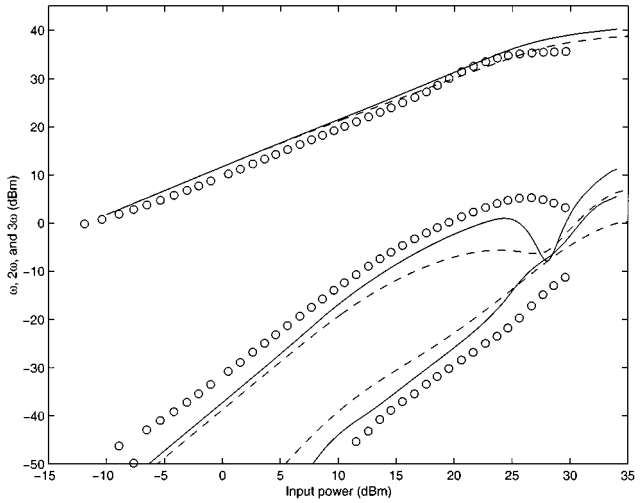

Fig. 20. Comparison of fundamental, second harmonic, and third harmonic power response of a power amplifier for the new electro-thermal model (solid lines), MET model (dashed lines), and measured results (circles).

Knot-optimized two-dimensional (2-D) TPS representations have been used to extract the charges by integrating the capacitances. Figs. 17 and 18 show the fitted C_{11} and C_{12}, respectively. The bottom portion of Fig. 18 zooms into the low $V_{\rm DS}$ region to highlight the fit. The solid lines are the TPS fitted data, while the circles are values extracted from the small-signal fit and augmented by extrapolation in regions where data is unavailable. $V_{\rm GS}$ ranges from 4 to 6.25 V in steps of 0.25 V. The TPS extracted gate charge is given in Fig. 19. A similar procedure is used to extract the drain charges by integrating C_{21} and C_{22}.

V. Amplifier Simulations and Comparisons With Measured Performance

A power amplifier was designed with a fully balanced input and output matching network [19] using microstrip transmission lines. The amplifier was designed to work at 945 MHz and is biased for class-AB operation at a $V_{\rm DS}$ of 20 V, an $I_{\rm DSS}$ of 76 mA, a $T_{\rm sub}$ of 35 °C, and a $T_{\rm dev}$ of 60 °C. The amplifier was designed to have a gain of 11.7 dB and an input 1-dB compression point of +26 dBm. The amplifier was simulated using the full electro-thermal model in ADS. For comparison purposes, the amplifier was also simulated using the Motorola MET model [9]. The experimentally determined value of $R_{\rm th}$ was used in the MET model simulations. The amplifier was then built and tested, and simulated and measured results were compared.

Fig 20 shows the comparison between the simulated (solid lines), measured (circles), and MET model (dashed lines) fundamental, second harmonic, and third harmonic response of the power amplifier. The measured amplifier gain is 11.7 dB and the input 1-dB compression point is at +24 dBm. From Fig. 20, it can be seen that the model does a good job in predicting the power harmonics. The MET model also does a good job in pre-

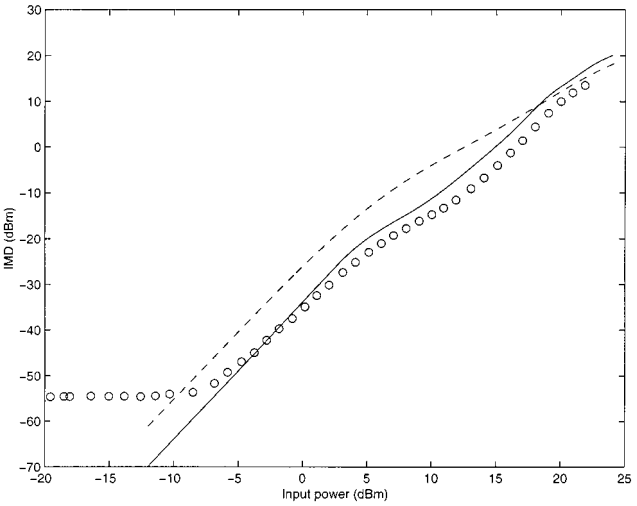

Fig. 21. Comparison of two-tone IMD response of a power amplifier for the new electro-thermal model (solid lines), MET model (dashed lines), and measured results (circles).

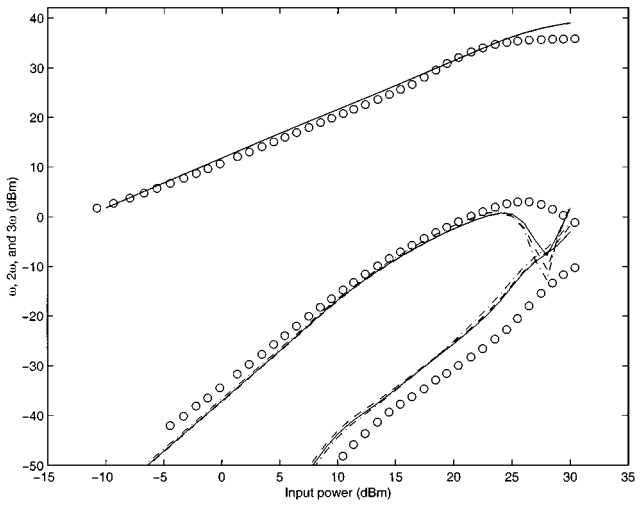

Fig. 22. Comparison of fundamental, second harmonic, and third harmonic power response of a power amplifier for charges of 60 °C (sold lines), 90 °C (dashed line), and 105 °C (dashed–dotted lines), respectively, compared with measured results (circles).

dicting the amplifier behavior after the experimentally determined thermal resistance value was used.

Discrepancies appear at higher power levels where the model predicts a P1dB to be 2 dBm higher and further predicts a sweet spot in the second harmonic at an input power level below what the measurements give. At these higher power levels, the model goes out of range and relies more on the extrapolated data regions (those regions that are inaccessible due to cooling limitations of the iso-thermal measurement technique) both in $V_{\rm GS}$ and $V_{\rm DS}$. This is confirmed by looking at the time-domain dynamic load line of the amplifier for different power levels. At higher power levels, a larger portion of the load line goes through the extrapolated regions. In the absence of greater substrate cooling, pulsed dc and pulsed RF can be used to obtain data in these regions.

A two-tone intermodulation test was performed on the amplifier at 945 and 946 MHz. Fig. 21 shows the $2\omega_2-\omega_1$ power as a function of input power. The solid line is the simulated IMD, the circles are measured, while the dashed line is the IMD obtained from the MET model. Clearly, the developed electro-thermal model does a very good job and performs comparatively better than the MET model. IMD data below -10 dBm of input power hits the noise floor of the measurement equipment.

A. Effect of Temperature-Dependent Charge

While the electro-thermal model presented relied on temperature dependent current, the 60 °C C_{12} and C_{22} were used to extract the temperature-independent charge. In order to examine the impact of the temperature variation of charge, a 90 °C and 105 °C charge representation is generated and used for amplifier simulations, respectively. Fig. 22 shows the obtained fundamental, second harmonic, and third harmonic power response for 60 °C (sold lines), 90 °C (dashed line), and 105 °C (dashed–dotted lines) charge representations, respectively. Measured data is indicated with circles. Note that, for the measured data, $T_{\rm dev}$ is 60 °C at low input powers (-10–0 dBm). However, as input power is further increased, $I_{\rm DSS}$ and $T_{\rm dev}$ increase dynamically due to the class-AB biasing of the LDMOSFET such that $T_{\rm dev}$ is 130 °C at $+30$ dBm of input power.

From Fig. 22, it can be seen that the higher temperature simulations show a deeper sweet spot in the second harmonic. The sweet spot is still at an input power level below what the measurements give. This sweet spot has been found to be very sensitive to the gate parasitic inductance L_g. However, it is clear that the model discrepancy from measured data at these higher powers is not due to the use of temperature-independent charge in spite of $T_{\rm dev}$ increasing by 70 °C. Hence, reduction in model accuracy at higher powers is primarily caused by the use of extrapolated data in high bias regions due to limitations in the data-acquisition scheme.

VI. Conclusion

We have presented a technique using iso-thermal *IV*s for the electro-thermal modeling of LDMOSFETs that bypasses the use of pulsed *IV*s and pulsed RF measurements. Iso-thermal *IV*s have been compared with hot- and cold-biased pulsed *IV*s demonstrating that there is indeed some low-frequency dispersion in LDMOSFETs. The technique using iso-thermal microwave measurements has been demonstrated for the extraction of temperature-dependent small-signal parameters. The conductance g_d and capacitances C_{12} and C_{22} are found to be relatively temperature independent.

Knot optimized 3-D TPSs have been used to represent the drain current. Gate and drain charges are represented using the same TPS technique, but are modeled to be temperature independent. The electro-thermal model has been programmed in ADS and has been used to simulate a power amplifier. The model is able to do a very good job in predicting power harmonics and two-tone IMD power-amplifier performance. The model matches and, in some cases, exceeds the existing MET

model. Limitations on substrate cooling limit data acquisition at higher bias values and, hence, the model accuracy is reduced at higher powers where the model relies more on extrapolated data.

REFERENCES

[1] G. Heftman, "GaAs, MOS, bipolar vie for power applications," *Microwaves RF*, vol. 37, no. 7, pp. 31–39, July 1998.

[2] C. P. Dragon, W. R. Burger, B. Davidson, E. Krvavac, N. Dixit, and D. Joersz, "High power RF-LDMOS transistors for base station applications," *R. F. Des.*, pp. 20–26, Mar. 2000.

[3] P. Khandelwal, M. Trivedi, K. Shenai, and S. K. Leong, "Thermal and package performance limitations in LDMOSFET's for RFIC applications," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 575–585, May 1999.

[4] J. M. Collantes, J. J. Raoux, R. Quere, and A. Suarez, "New measurement-based technique for RF LDMOS nonlinear modeling," *IEEE Microwave Guided Wave Lett.*, vol. 8, pp. 345–347, Oct. 1998.

[5] J.-P. Tayssier, P. Bouysse, Z. Ouarch, D. Barataud, T. Peyretaillade, and R. Quere, "40-GHz/150-ns versatile pulsed measurement system for microwave transistor isothermal characterization," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 2043–2052, Dec. 1998.

[6] C. de Boor, *A Practical Guide to Splines*. Berlin, Germany: Springer-Verlag, 1978.

[7] G. Bischoff and J. P. Krusius, "Technology independent device modeling for simulation of integrated circuits for FET technologies," *IEEE Trans. Computer-Aided Design*, vol. CAD-4, pp. 99–110, Jan. 1985.

[8] R. R. Daniels, A. T. Yang, and J. P. Harrang, "A universal large/small signal 3-terminal FET model using a nonquasi-static charge-based approach," *IEEE Trans. Electron Devices*, vol. 40, pp. 1723–1729, Oct. 1993.

[9] W. R. Curtice, J. A. Pla, D. Bridges, T. Liang, and E. E. Shumate, "A new dynamic electro-thermal nonlinear model for silicon RF LDMOS FETs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, 1999, pp. 419–422.

[10] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 448–456, May 1980.

[11] "The RF MOSFET line: RF power field effect transistor: N-channel enhancement-mode lateral MOSFET," Motorola, Denver, CO, Semiconduct. Tech. Data Rep., 1999.

[12] S. Akhtar and P. Roblin, "B-spline based, large-signal DC and microwave-model for SOI-MOSFETs," in *Analog Integrated Circuits and Signal Processing*. Norwell, MA: Kluwer, Nov. 2000, vol. 25.

[13] S. Akhtar, P. Roblin, S. Lee, and J. Strahler, "Iso-thermal DC and microwave characterizations of power RF silicon LDMOSFETs," *IEEE Trans. Electron Devices*, vol. 48, pp. 2785–2789, Dec. 2001.

[14] P. Roblin, S. Akhtar, and J. Strahler, "New nonquasi-static theory for extracting small-signal parameters applied to LDMOSFETs," *IEEE Microwave Guided Wave Lett.*, vol. 10, pp. 322–324, Aug. 2000.

[15] J.-P. Raskin, R. Gillon, J. Chen, D. Vanhoenacker-Janvier, and J.-P. Colinge, "Accurate SOI MOSFET characterization at microwave frequencies for device performance optimization and analog modeling," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1017–1025, May 1998.

[16] S. Akhtar, "Modeling of RF power transistors for power amplifier design," Ph.D. dissertation, Dept. Elect. Eng., The Ohio State Univ., Columbus, OH, June 2000.

[17] ——, "Highly accurate large-signal microwave-model for SOI-MOSFET's," Master's thesis, Dept. Elect. Eng., The Ohio State Univ., Columbus, OH, 1996.

[18] P. Roblin, S. C. Kang, and W. R. Liou, "Improved small-signal equivalent circuit model and large-signal state equations for the MOSFET/MODFET wave equation," *IEEE Trans. Electron Devices*, vol. 38, pp. 1706–1718, Aug. 1991.

[19] G. Gonzalez, *Microwave Transistor Amplifiers*. Englewood Cliffs, NJ: Prentice-Hall, 1984.

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