Typical Design Problems and Tips of Fabrication

for EE710/EE723

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Chapter 1

Problems about Layout

1.1 Don’t know how to generate layout

To generate layout, follow the following steps:

- In your Schematic window, deactivate lumped components, such as Chip Resistors, Capacitors and Vias
- Select ”Layout–>Generate/Update Layout” from your Schematic window
- Click OK
- The Layout window will appear then, you may edit your layout then

1.2 Forget to add top ground plane

To achieve highly efficient fabrication, each group is suggested to add top ground plane into layout. Go to the following link to learn several steps of adding ground plane.

http://www.eleceng.ohio-state.edu/ads/grounds.html

- Create a ”Bound” Shape
- Create a ”Cond” Shape
- Create Clearance
- Select Cut Shapes

1.3 Typical Problems in Layout

As shown in Figure 1.1, students often have the following three kinds of errors in their layouts.

Figure 1.1: Figures of Typical Problems

- In either A or B, the microstrip line is too close to the boundary that short connection to the bottom ground may happen.
- In C, the SMA connector does not touch or not fully connect with the microstrip line.
- In D, the space between microstrip line and boundary is too small. The width of the whole boundary is also too narrow.
Chapter 2

Tips of Fabrication

2.1 Procedure of Fabrication

Generate *.gbr files from Layout window

- In your Schematic window...

Figure 2.1: Attentions to Rubout