Accelerated Design Methodology for Dual-Input Doherty Power Amplifiers

Chenyu Liang, Student Member, IEEE, Patrick Roblin, Senior Member, IEEE, and Yunsik Hahn, Student Member, IEEE

Abstract—A novel design theory and the methodology are presented for dual-input Doherty power amplifiers (DPAs) in which the auxiliary transistor does not fully turn off at backoff power. Given the input parameters selected by the PA designer, a Doherty load modulation behavior is exactly implemented at the current-source reference planes of the transistors by solving for the characteristic impedance of the Doherty quarter-wave transformer and the common load. The Doherty output combiner at the package reference plane that sustains the desired dual-input DPA performance is then synthesized using nonlinear embedding and exactly implemented with a lossless and reciprocal circuit. The new analytic DPA design theory also provides an expanded design space, which facilitates the selection of the optimal design based on the gain, linearity, and efficiency tradeoff. The design methodology is implemented in a software program to enable the automatic design of a dual-input DPA prototype at the package reference planes within 24 s. To validate the theory and the design methodology, a 2-GHz dual-input asymmetric DPA is fabricated and measured. When excited with a 20-MHz local thermal equilibrium (LTE) signal with 9.55-dB peak-to-average power ratio (PAPR), the DPA achieves an average power-added efficiency (PAE) of 51.6% with an adjacent-channel-power-leakage ratio (ACLR) of −47.1 dBc after linearization.

Index Terms—Doherty power amplifiers (DPAs), nonlinear embedding.

I. INTRODUCTION

DOHERTY power amplifiers (DPAs) have been widely adopted in base stations for signals with high peak to average power ratio (PAPR). The conventional Doherty load modulation behavior relies on a quarter-wave (λ/4) transformer and a common load connecting the main and auxiliary amplifiers. The load modulation mechanism dynamically changes the load impedances seen by the transistors in order to maintain a constant drain voltage swing for the main amplifier from the backoff power to peak power levels. As a result, a high efficiency is achieved at both peak and backoff power [1]–[14]. At microwave frequencies, the nonlinear capacitances and parasitic presented in a realistic transistor strongly impact its performances at the package reference planes. Multi-harmonic load–pull is the most commonly used technique in DPA design. Output matching networks, offset lines, and a quarter-wave transformer are then used to implement the Doherty combiner [4]. Recently, a power amplifier (PA) combiner synthesis technique used for designing DPAs at the package reference planes has been proposed and demonstrated in [15]–[17] and [19]. The PA fundamental output combiner is treated as a lossy and reciprocal two-port network realized with a lossless three-port network terminated with a resistive load. The Z parameters of the two-port network are derived by applying the optimal impedances obtained from load–pull measurements or simulations. The desired phase offset of the DPA at backoff and peak power is numerically found. It is usually different from the 90° phase offset used in the conventional DPAs. Similarly, the technique is also applied to design outphasing power amplifiers in [17] and [20]. This combiner synthesis technique has the advantage of simplifying the design process and fully utilizing the transistors’ capability for a dual-input DPA. However, for a single input DPA, an approximate design is required where the phase offset at the peak is typically taken the same as the phase offset at backoff. Alternatively, the approximate combiner reported in [26, Appendix C] could be used.

Instead of performing multi-harmonic load–pull simulations or measurements, an alternative way of designing DPA using a nonlinear embedding device model has been proposed by Jang et al. [21], [22]. It is a model-based approach to designing PAs by nonlinear embedding [27]. The optimal DPA prototype that provides the desired performance is first implemented at the transistors’ current-source reference planes. The nonlinear embedding device model is capable of predicting the corresponding multi-harmonic load impedances at the package reference planes. These are then converted from complex to real values by using offset lines and impedance transformers. The DPA design method discussed in [21] and [22] provides an effective approach that eliminates the time-consuming multi-harmonic load–pull and source–pull measurements or simulations while still delivering an optimal PA performance. However, the design of the offset lines and the impedance transformers in [21] and [22] requires a tuning process to implement the desired ideal Doherty load modulation at the package reference planes.

The motivation for this paper is to provide a rigorous and systematic design process for dual-input Doherty PAs. This is achieved among other things by combining the nonlinear embedding approach in [21] and [22] with a combiner...
synthesis technique at the package references planes similar to the one introduced in [15]. Furthermore, a novel generalized Doherty PA theory at the current-source reference planes is developed. The new DPA theory presented in this work does not assume that the auxiliary PA completely turns off at backoff power. Besides differing from the conventional DPA theory, the fundamental voltages seen by the main PA can vary to some extent from backoff power to peak power to account for the IV knee voltage variation with the gate voltage. The resulting theory makes it possible to directly design a DPA prototype at the current-source reference planes given the design parameters selected by the PA designer such as the operating frequency, maximum drain voltage, maximum drain current, and Doherty asymmetry power ratio. The new approach presented in this work is based on the generalized DPA theory, which yields a direct analytic DPA design solution. The updated approach eliminates the needs for solving the transcendental equation reported in [34], which required a time-consuming iterative numerical process. As a result, the proposed algorithm based on the new approach in this work has significantly reduced the design duration from 95 s reported in [34] to currently 24 s. A MATLAB graphical user interface (GUI) for the algorithm has been also developed to promote and facilitate the design approach. Furthermore, a large design space is enabled by the generalized theory as it provides additional degrees of freedom permitting to explore the gain-linearity-efficiency tradeoff in the DPA design. Once the DPA prototype with the desired performance at the package reference plane, which executes a few harmonic balance simulations. The program automatically produces a functional DPA prototype at the current-source reference planes. This greatly simplifies the design process and enables the PA designer to more efficiently explore the large DPA design space.

This paper is organized as follows. In Section II, the novel generalized DPA design theory is introduced. The design methodology and simulation results for the DPA prototype are discussed in Section III. The DPA demonstrator circuit is implemented and fabricated as presented in Section III. The continuous-wave (CW) measurements and the modulated signal measurements of the DPA demonstrator circuits are reported in Section IV. Finally, conclusions are drawn in Section V.

II. NOVEL GENERALIZED DPAs DESIGN THEORY

A diagram for a prototype DPA at the current-source reference plane is presented in Fig. 1. The main and auxiliary transistors are represented by two ideal current sources. They are connected to a common load $R_L$ using a $\lambda/4$ transformer with a characteristic impedance of $Z_T$. The load impedances seen by the main and auxiliary transistors are both real ($R_m$ and $R_a$) for class-B, F, or C operation at the fundamental frequency. Therefore, the fundamental currents and voltages of the main transistor at peak and backoff power are defined as

$$I_{mp} = |I_{mp}|, \quad V_{mp} = |V_{mp}|,$$
$$I_{mb} = |I_{mb}|, \quad V_{mb} = |V_{mb}|. \quad (1)$$

Due to the $\lambda/4$ transformer, a 90° phase shift is introduced between the fundamental currents flowing through the main and auxiliary transistors. The fundamental currents and voltages of the auxiliary transistor at peak and backoff power are defined as

$$I_{ap} = -j|I_{ap}|, \quad V_{ap} = -j|V_{ap}|,$$  
$$I_{ab} = -j|I_{ab}|, \quad V_{ab} = -j|V_{ab}|. \quad (2)$$

The subscript $p$ refers to the peak power level, e.g., $I_{mp}$ is the fundamental current flowing through the main transistor at the peak power. Similarly, the subscript $b$ refers to the backoff power level, e.g., $I_{mb}$ is the fundamental current flowing through the main transistor at the backoff power.

At the junction point as denoted in Fig. 1, the amplitude of the fundamental drain voltage seen by the main transistor is given by

$$|V_m| = |I_m|R_m. \quad (3)$$

The impedance seen by the main transistor $R_m$ is derived by applying the $\lambda/4$ transformer equation and is given by

$$R_m = \frac{Z_T^2}{R_m}. \quad (4)$$

The amplitude of voltage $|V_L|$ across the common load $R_L$ is calculated by

$$|V_L| = |I_m^\prime|R_m^\prime = \left(|I_m| + |I_a|\right)R_L. \quad (5)$$

The impedance $R_m^\prime$ is given by

$$R_m^\prime = R_L \left(1 + \frac{|I_a|}{|I_m|}\right). \quad (6)$$

Plugging (4)–(6) into (3) and applying the ABCD parameters of the $\lambda/4$ transformer, $|V_m|$ is given by

$$|V_m| = -jZ_TR_e + |I_m|\frac{Z_T^2}{R_L}. \quad (7)$$

The novel DPA theory proposed in this work does not assume the auxiliary transistor turns completely off at the
backoff power level. This implies a nonzero auxiliary backoff fundamental current |I_{ab}|. The amplitude of the fundamental voltages |V_{mp}| and |V_{mb}| in (7) are then given by
\[ |V_{mb}| = -j Z_T |I_{ab}| + |I_{mb}| \frac{Z_T^2}{R_L} \]
\[ |V_{mp}| = -j Z_T |I_{ap}| + |I_{mp}| \frac{Z_T^2}{R_L} = \nu |V_{mb}| \]
where \( \nu = 1 \) for ideal transistors with zero knee voltages. Solving (8), a generalized expression for the characteristic impedance \( Z_T \) of the \( \lambda/4 \) transformer and the common load \( R_L \) is obtained
\[ Z_T = \frac{|V_{mb}| |I_{mp}| - |V_{mp}| |I_{mb}|}{|I_{mb}| |I_{mp}| - |I_{mp}| |I_{mb}|} \]
\[ R_L = \frac{(|V_{mb}| |I_{mp}| - |V_{mp}| |I_{mb}|)^2}{(|I_{mb}| |I_{mp}| - |I_{mp}| |I_{mb}|)(|V_{mb}| |I_{mp}| - |V_{mp}| |I_{mb}|)} \] (9)

The amplitude of the voltage across the common load at peak power \( |V_L| \) is equal to \( |V_{ap}| \), which is given by
\[ |V_{ap}| = |I_{mp}| |Z_T| \] (11)

Based on (9) and (11), \( |V_{ap}| \) is further expressed by
\[ |V_{ap}| = |I_{mp}| \frac{|V_{mb}| |I_{mp}| - |V_{mp}| |I_{mb}|}{|I_{mb}| |I_{mp}| - |I_{mp}| |I_{mb}|} \] (12)

The \( \lambda/4 \) transformer in the DPA prototype behaves as an impedance inverter, which determines \( |I_{mp}|/|I_{mb}| = |V_{ap}|/|V_{ab}| \). Equation (12) then becomes
\[ |V_{mb}| |I_{mp}| - |V_{mp}| |I_{mb}| = |V_{ab}| |I_{ap}| - |V_{ap}| |I_{lab}| \] (13)

Equation (13) divided by \( |I_{ap}| \) yields the transcendental equation derived in [34], which was numerically solved. However, in this paper, the solution for the unknown fundamental voltages and currents is obtained analytically. The asymmetry peak power ratio between auxiliary and main PAs in a DPA is defined to be [22]
\[ n = \frac{P_{ap}}{P_{mp}} = \frac{|V_{ap}| |I_{ap}|}{|V_{mp}| |I_{mp}|} = \frac{1}{\gamma_{vp}\gamma_{ip}} \] (14)

where \( P_{ap} \) and \( P_{mp} \) refer to the fundamental peak powers delivered by the auxiliary and main PAs, respectively. The parameters \( \gamma_{vp} = |V_{mp}|/|V_{ap}| \) and \( \gamma_{ip} = |I_{mp}|/|I_{ap}| \) are defined to be the fundamental drain voltage and current ratios between the main and auxiliary PAs at peak power [22, Appendix I]. Based on (13) and (14), the asymmetry peak power ratio \( n \) can be rewritten as
\[ n = \frac{K - \nu}{\nu(1 - \delta K)} \] (15)

with \( K = |I_{mp}|/|I_{mb}| \) and \( \delta = |I_{ab}|/|I_{ap}| \). It is worth mentioning that in the conventional Doherty PA theory in which the auxiliary PA is fully turned off at backoff power (\( \delta = 0 \)) and the fundamental drain voltage for the main PA \( |V_{ma}| \) is maintained constant from backoff to peak power (\( \nu = 1 \)), as a result, the asymmetry peak power ratio reduces to \( n = K - 1 \).

The output backoff range (OBO) of the DPA is calculated by using the ratio between the overall peak power \( P_{op} \) and the overall backoff power \( P_{ob} \) of the DPA. Based on (13) and (15), the OBO is given by
\[ OBO = K^2 = \left( \frac{\nu(n+1)}{1+n\nu} \right)^2 \] (16)

For the conventional DPA theory with \( \delta = 0 \) and \( \nu = 1 \), the OBO simplifies to \((n + 1)^2\).

In summary, the generalized DPA design theory establishes the relationships between the eight voltage and current parameters (|V_{mp}|, |V_{mb}|, |I_{mp}|, |I_{mb}|, |V_{ap}|, |V_{ab}|, |I_{ap}|, and |I_{lab}|) and the six design parameters (|V_{max}|, |I_{max}|, \( n \), \( \gamma_{vp} \), \( \delta \), and \( \nu \)). Note that in a DPA, the maximum drain voltage \( V_{max} \) is taken to be approximately equal to twice of the amplitude of fundamental drain voltage at peak power for the auxiliary PA |V_{ap}|. |V_{max}| \approx 2|V_{ap}|\). Similarly, the maximum drain current \( I_{max} \) is approximately equal to twice of the amplitude of fundamental current at peak power for the auxiliary PA |I_{ap}|. |I_{max}| \approx 2|I_{ap}|\).

The eight voltage and current parameters are used to determine the Doherty load modulation scheme and to provide the required characteristic impedance of the \( \lambda/4 \) transformer \( Z_T \) and the common load \( R_L \). The load impedances \( (R_{mp}, R_{mb}, R_{ap}, \text{and } R_{ab}) \) seen by the main and auxiliary PAs at peak and backoff are also determined, respectively. The corresponding input-RF voltages for the main and auxiliary PAs at peak and backoff can be extracted by using the embedding device model at the current-source reference planes in [22]. A DPA prototype at the current-source plane is then established. In Section III, a DPA design methodology based on this theory is presented and illustrated with design examples.

### III. Design Methodology and Design Space for Dual-Input Doherty PAs

In this section, a methodology for designing DPA prototypes at the current-source reference planes will be first discussed. An automatic DPA design algorithm is then implemented in MATLAB using this methodology. The desired multi-harmonic currents and voltages are predicted at the package reference planes using the embedding device model reported in [21] and [22]. The input matching networks and output combiner are designed based on the multi-harmonic currents and voltages at the package reference planes. Simulation results for multiple DPA prototypes generated using this automatic DPA design algorithm are presented to explore the design space and reveal the DPA gain-linearity-efficiency tradeoff. A DPA demonstrator circuit is then designed and built.

A DPA prototype at the current-source reference plane is to be implemented based on Fig. 2(a). The main PA is operated in ideal class-F with the second and third harmonic currents terminated by ideal short and open circuits, respectively. The auxiliary PA is operated in ideal class-C with the second and third harmonic currents both terminated with ideal short circuits. The DPA prototype is established with the class-F (main) and class-C (auxiliary) PAs connected with the \( \lambda/4 \) transformer and the common load.
A. Design Methodology

**Step 1:** The operating frequency $f_0$, the maximum drain voltage $V_{\text{max}}$, the maximum drain current $I_{\text{max}}$, the desired asymmetry peak power ratio $n$ (approximately 2 for 9.54-dB OBO), the main-to-auxiliary peak voltage ratio $\gamma_{\text{vp}}$ (typically between 1/n and 1), the auxiliary backoff-to-peak current ratio $\delta$ (0 for the ideal case), and the main peak-to-backoff voltage ratio $\nu$ (1 for zero knee voltage IV) are the input parameters set by the PA designer.

Given the above design input parameters selected by the PA designer, the eight unknown voltage and current parameters ($|V_{\text{mp}}, |V_{\text{mb}}, |I_{\text{mp}}, |I_{\text{mb}}, |V_{\text{ap}}, |V_{\text{ab}}, |I_{\text{ap}}, \text{and } |I_{\text{ab}}|$) can be then determined. The OBO and $K$ factor are calculated using (16). For the auxiliary PA, the fundamental drain voltage and current at peak power are selected as $|V_{\text{ap}}| = V_{\text{max}}/2$ and $|I_{\text{ap}}| = I_{\text{max}}/2$, respectively. The fundamental drain current and voltage for the auxiliary PA at backoff power is given by $|I_{\text{ab}}| = \delta|I_{\text{ap}}|$ and $|V_{\text{ab}}| = |V_{\text{ap}}|/K$, respectively. For the main PA, the fundamental drain voltages at peak and backoff powers are obtained from $|V_{\text{mp}}| = \gamma_{\text{vp}}|V_{\text{ap}}|$ and $|V_{\text{mb}}| = |V_{\text{mp}}|/\nu$, respectively. The fundamental drain current at peak power is obtained using $|I_{\text{mp}}| = \gamma_{\text{vp}}|I_{\text{ap}}|$, with $\gamma_{\text{vp}} = \gamma_{\text{vp}}/n$. The fundamental drain current for the main PA at backoff power is then given by $|I_{\text{mb}}| = |I_{\text{mp}}|/K$.

**Step 2:** Single-transistor (main and auxiliary) simulations as shown in Fig. 2(b) are conducted to find the RF-input voltages for the main and auxiliary PAs, which deliver the fundamental voltages and currents established in Step 1. These are performed by the four independent single-transistor simulations shown in Fig. 2(b) by sweeping the input-RF voltages $|V_{\text{GS,m}}|$ or $|V_{\text{GS,a}}|$ and using interpolation. For these simulations, the main and auxiliary drain biases are set to be $V_{\text{DD,m}} = |V_{\text{mp}}| + V_{\text{on,m}}$ and $V_{\text{DD,a}} = |V_{\text{ap}}| + V_{\text{on,a}}$, respectively, with $V_{\text{on,m}/a}$ representing the IV knee voltages. The main and auxiliary gate biases $V_{\text{GG,m/a}}$ are set around and below the device threshold voltage $V_T$, respectively. The resistive loads used are the targeted impedances ($R_{\text{mp}}, R_{\text{mb}}, R_{\text{ap}}, \text{and } R_{\text{ab}}$) seen by the main and auxiliary PA at peak and backoff, respectively.

**Step 3:** The DPA prototype can be verified at the current-source reference planes as shown in Fig. 2(c). The required input-RF voltages determined in Step 2. This verification is performed in Step 3 with the embedding device model, which also provides the voltages and currents at the package reference planes that sustains this mode of operation. The main and auxiliary input-RF voltages between the backoff and peak power levels are simply selected to vary linearly as predicted by the ideal Doherty theory for constant conductance transistors [22].

**Step 4:** The DPA two-port combiner network at the package reference planes is designed and the input phase offsets are determined. The DPA operation is verified at the package reference plane as shown in Fig. 2(c). The two-port combiner network generated by nonlinear embedding is usually not realizable by a reciprocal and lossless three-port network terminated by a resistor. However, a DPA with the same power and efficiency at peak and backoff can be obtained by synthesizing a reciprocal and lossless three-port combiner network using
Step 1. Set $V_{\text{max}}$, $I_{\text{max}}$, $n_{\text{tap}}$, $\delta$ and $\psi$. Calculate $Z_T$, $R_L$ from (9) and (10) and obtain the optimal load resistance $R_{mp}$, $R_{mb}$, $R_{ap}$ and $R_{ab}$.

Step 2. Select $|V_{\text{DD,}m}| - |V_{\text{mp}}| + |V_{\text{on,}m}|$. Set $R_{mp}$ and $R_{mb}$ and sweep $|V_{\text{GS,}m}|$ to obtain optimal $|V_{\text{GS,}mp}|$ and $|V_{\text{GS,}mb}|$. Select $|V_{\text{DD,}a}| = |V_{\text{ap}}| + |V_{\text{on,}a}|$. Set $R_{ap}$ and $R_{ab}$ and sweep $|V_{\text{GS,a}}|$ to obtain optimal $|V_{\text{GS,ap}}|$ and $|V_{\text{GS,ab}}|$.

Step 3. Verify the Doherty PA prototype at the current-source ref. plane and perform the non-linear embedding to the package ref. planes.

Step 4. Design the output harmonic matching. Calculate the $S$ parameters of the output combiner using (20)-(22). Synthesize the combiner circuits at the package ref. plane.

Step 5. Design the input matching network.

The DPA design is finished.

Fig. 4. Design flowchart for a DPA circuit based on the methodology in this work.

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a technique similar to that reported in [15]–[17]. Given the desired DPA operations at the current-source reference plane at both backoff and peak power in Fig. 2(a), the fundamental drain voltages and currents at the package reference planes. The subscript $p$ refers to the package reference plane.

The $Z$ parameters of the two-port combiner network at the fundamental frequency are obtained from

$$
Z_P = \begin{bmatrix}
Z_{11,P} & Z_{12,P} \\
Z_{21,P} & Z_{22,P}
\end{bmatrix} = Z_P \begin{bmatrix}
I_{mp,P} & I_{mb,P} \\
I_{ap,P} & I_{ab,P}
\end{bmatrix}.
$$

(19)

Solving (19), the $Z$ parameters are given by

$$
Z_{11,P} = \frac{(V_{mp,P} - V_{mb,P})}{\Delta},
$$

$$
Z_{12,P} = \frac{(V_{mb,P} - V_{mp,P})}{\Delta},
$$

$$
Z_{21,P} = \frac{(V_{ap,P} - V_{ab,P})}{\Delta},
$$

$$
Z_{22,P} = \frac{(V_{ab,P} - V_{ap,P})}{\Delta},
$$

with $\Delta = I_{mp,P}I_{ab,P} - I_{mb,P}I_{ap,P}$. (20)

The two-port network must be reciprocal, which requires $Z_{12,P} = Z_{21,P}$. Based on (19), the following constrain is derived:

$$
e^{j(\psi_b + \psi_p)} = \gamma
$$

with

$$
\gamma = \frac{|V_{mp,P}|I_{mb,P}|e^{j\phi_{mp}} - |V_{mb,P}|I_{ap,P}|e^{j\phi_{ab}}}{|V_{mb,P}|I_{mp,P}|e^{j\phi_{mp}} - |V_{mp,P}|I_{mb,P}|e^{j\phi_{ab}}}. \tag{21}
$$

Equation (21) indicates that the relationship between the input phase offset $\psi_b$ at backoff power and $\psi_p$ at peak power is given by

$$
\psi_b + \psi_p = \angle \gamma. \tag{22}
$$

The reciprocal two-port network shown in Eq. 2(c) consists of a lossless three-port network terminated with a 50-$\Omega$ load. Applying a well-known criterion mentioned in [15] and derived in [31], which enforces the losslessness of the three-port network, the two-port $Z$ parameters must verify:

$\Re^2[Z_{12}] = \Re[Z_{11}]/\Re[Z_{22}]$. The input phase offsets $\psi_b$ and $\psi_p$ which satisfy this criterion can then be numerically computed similar to [16] and [17]. As shown in Fig. 3, the difference $\Re^2[Z_{12}] - \Re[Z_{11}]/\Re[Z_{22}]$ is numerically plotted versus the input phase offset at backoff power $\psi_b$. Any solution of the input phase offset angle can be selected as long as it satisfies this criterion. In this work, the first solution ($\psi_b = 98.7^\circ$) as indicated by the red hexagon is selected for the design example in this section. Finally, the two-port network at the fundamental frequency connected with the two transistor models is obtained from (20). It is worth mentioning
that the input phase offsets $\psi_p$ and $\psi_b$ for the DPA at the package reference planes are no longer equal to 90°. The input phase offsets between backoff and peak are linearly varied with the incident power level. The output harmonic matching circuits are designed based on the optimal harmonic impedances predicted by the embedding device model. This will be discussed in detail in Section IV.

Step 5: Given the input fundamental impedances predicted by the embedding device model, a conjugate matching is performed at the fundamental frequency to maximize the gain. The phase of the input second harmonic is also predicted by the embedding device model and used to further maximize the drain efficiency of the DPA. To conclude, the flowchart used to explain the design of DPA prototypes at the current-source reference and package reference planes is presented in Fig. 4.

B. Parametric Sweep Simulations for Doherty PA Prototypes

The design methodology proposed in this work can be used to facilitate the DPA design process. In this work, the design algorithm was implemented in a MATLAB code for the automatic design of DPAs. It is also noted that an alternative implementation approach by Keysight Advanced Design Systems (ADS) and SystemVue Co-Simulation is proposed in [23]. The MATLAB code calls five harmonic balance simulations that are performed by running ADS netlists under script control. A MATLAB GUI as shown in Fig. 5 was created for Steps 1–3 in Fig. 4 to facilitate the design of DPA prototypes at the package reference planes based on the input parameters selected by the PA designer. A DPA design takes typically 24 s to complete on a laptop computer, which includes the calculations from Step 1 to Step 2 in Fig. 4.

It takes about 31 s to obtain the performance verification for the DPA prototype by sweeping the input RF voltages, which corresponds to the Step 3 in Fig. 4. The input design parameters outlined by the red box in Fig. 5 includes the operating frequency $f_0$, the maximum drain voltage $V_{\text{max}}$, the maximum drain current $I_{\text{max}}$, the desired asymmetry peak power ratio $n$, the main-to-auxiliary PA peak voltage ratio $\gamma_{vp}$, the auxiliary peak-to-back current ratio $1/\delta$, and the main peak-to-backoff voltage ratio $\nu$. The output parameters for the DPA prototype outlined by the blue box are the calculated $\lambda/4$ characteristic impedance $Z_T$, the common load $R_L$, and the input-RF voltages. The results shown in the GUI are listed in the left side. The load lines at the current-source reference planes seen by the main and auxiliary PAs are presented in Fig. 5(a) and (b), respectively. The Doherty fundamental impedance modulation trajectories seen by the main and auxiliary PAs are illustrated in Fig. 5(c) and (d), respectively. The drain voltage and current waveforms are shown in Fig. 5(e) and (f), respectively. The drain efficiency and gain predicted by the DPA prototype at the package reference plane are shown in Fig. 5(g). After the nonlinear embedding process, the S-parameters of the output combiner circuits at the package reference plane are shown in Fig. 5(h). The input fundamental and second harmonic impedance are also indicated in Fig. 5(h). The total output power and the output power for main and auxiliary PAs are plotted in Fig. 5(i) versus input power to present the AM/AM behavior of the designed DPA prototype. The DPA prototype at the current-source reference planes used for the GUI is depicted in Fig. 5(j) with the two ideal current sources connected with the $\lambda/4$ transformer and the common load. Finally, the packaged DPA prototype is shown in Fig. 5(k) with the two package device models connected.
to select the peak fundamental drain voltage ratio between the main and auxiliary PA $\gamma_{vp}$ to be between 1 and 1/n. In this work, $\gamma_{vp} \approx 0.5$ (asymmetric dc drain bias) is adopted as it leads to a smaller full voltage swing seen by the main PA, which reduces the device trap activity and increases the backoff efficiency. By linearly sweeping $n$ from 2.05 to 3.05, the backoff efficiency drops while the gain becomes higher and more linear as illustrated in Fig. 6(a). Similar patterns are also observed in Fig. 6(b), where $\Delta V_m$ is varied from $-2$ to 2 V. To better visualize the dependence of the DPA performances upon $n$ and $\Delta V_m$, a variety of DPA figures of merit are presented in Fig. 7 in the 2-D design space provided by $n (1.7 < n < 2.7)$ and $\Delta V_m (-1.6 < \Delta V_m < 1.6)$. The efficiency, gain, and output power at backoff and peak power versus $n$ and $\Delta V_m$ are shown in Fig. 6(a)–(f), respectively. Fig. 6(g) and (h) shows the characteristic impedance $Z_T$ of the $\lambda/4$ transformer and the common load $R_L$, respectively. After the nonlinear embedding process, the S-parameters of the output combiner networks at the package reference planes are also obtained based on (19) and plotted in Fig. 6(i).

In summary, the asymmetry peak power ratio $n$ and the main PA voltage imbalance $\Delta V_m = V_{mp}(1 - \nu)$ provide a design space enabling a gain-linearity-efficiency tradeoff in DPA designs. The PA designer can then select the desired performance tradeoff accordingly. The 2-D design space created by sweeping $n$ and $\Delta V_m$ could also be beneficial to broadband DPA designs by utilizing the continuous mode presented in Fig. 7(i).

C. Design Example of a 2-GHz Dual-Input DPA Demonstrator Circuit

As discussed in Section III-B, the 2-D design space sustained by the asymmetry peak power ratio $n$ and the main PA voltage imbalance $\Delta V_m$ establishes a large design space with gain-linearity-efficiency tradeoff for DPA prototypes at the package reference planes. To validate the design methodology, a 2-GHz dual-input DPA demonstrator circuit is designed. It is worth mentioning that the analytic theory proposed in this work is able to yield the same DPA design obtained from the numerical solutions in [34]. To start with, $n = 1.78$, $\Delta V_m = 1.5$, $\delta = 0.015$, $|\gamma_{vp}| = 0.56$, $I_{max} = 2.1$ A, and $V_{max} = 60.0$ V are selected for the design. The OBO is equal to 9.4 dB. The values of the currents and voltages at the current-source reference planes, the intrinsic characteristic impedance of $Z_T$ for the $\lambda/4$ transformer and the common load of $R_L$, the associated RF-input voltage at peak and backoff power and dc bias values are all obtained and summarized as shown in Table I. A DPA prototype as shown in Fig. 2(a) is then established at the current-source reference planes. By simulating the DPA prototype at backoff and peak power levels, the voltages and currents at package reference planes are predicted using the embedding device model and are given by: $V_{imp,p} = -7.55 - j 13.74$ V, $V_{imp,p} = -2.43 - j 12.94$ V, $V_{ap,p} = -24.84 + j 7.50$ V, $V_{ab,p} = -8.63 + j 0.01$ V, $I_{mp,p} = -0.32 - j 0.93$ A, $I_{mp,p} = -0.28 - j 0.31$ A, $I_{ap,p} = -0.94 + j 0.52$ A, $I_{ab,p} = -0.015 + j 0.18$ A. The S-parameters at the fundamental frequency of the DPA output with harmonic filters and a two-port output combiner network.

This software program enables to quickly generate multiple DPA prototypes with different performances using parametric sweep simulations of the design parameters. The gain-linearity-efficiency tradeoff is observed as shown in Fig. 6 by sweeping two salient design input parameters: the asymmetry peak power ratio $n$ and the drain voltage imbalance of main PA $\Delta V_m$, where $\Delta V_m = V_{mp} - V_{imp} = V_{mp}(1 - \nu)$. In Fig. 6, a total of 22 DPA prototypes with distinctive performances are created and simulated. For these parametric sweep simulations, several initial design input parameters are selected. In all these simulations, an OBO = 9.54 dB is targeted as the desired Doherty backoff range. The maximum instantaneous current for auxiliary PAs $I_{max}$ is set to be 2.3 A, together with the maximum instantaneous voltage for auxiliary PAs $|V_{max}| = 60$ V. The fundamental voltage ratio between the main and auxiliary PA at peak power is set to be $\gamma_{vp} = 0.5$. The Doherty prototypes are all biased at the same condition: $V_{GG,m} = -2.9$ V, $V_{GG,a} = -4.1$ V, $V_{DD,m} = 16.5$ V, and $V_{DD,a} = 33$ V. It is noted that for asymmetric DPA designed with two identical device models, PA designers have the option...
Fig. 7. Figure of merits shown in the 2-D DPA design space established by sweeping the asymmetry peak power ratio \( n \) and the drain voltage imbalance of main PA \( \Delta V_m \). (a) Backoff efficiency. (b) Backoff gain. (c) Backoff output power. (d) Peak efficiency. (e) Peak gain. (f) Peak output power. (g) \( Z_T \) of \( \lambda/4 \) transformers. (h) Common load \( R_L \). (i) S-parameters of the output combiners at the package reference planes.

**TABLE I**

**DESIGN PARAMETERS FOR THE DUAL-INPUT DPA AT 2 GHz**

| \( V_{\text{max}} \) | \( I_{\text{max}} \) | \( r_i \) | \( \gamma_{\text{up}} \) | \( \delta \) | \( \nu \) | \( |V_{\text{mp}}| \) |
|-----------------|-----------------|--------|----------------|--------|--------|-----------------|
| 60.0 V          | 2.1 A           | 1.78   | 0.56           | 0.016  | 1.1    | 17.0           |
| \( |V_{\text{mb}}| \) | \( |I_{\text{mp}}| \) | \( |I_{\text{mb}}| \) | \( |V_{\text{up}}| \) | \( |V_{\text{bp}}| \) | \( |V_{\text{ab}}| \) | \( |I_{\text{pa}}| \) | \( |I_{\text{ab}}| \) |
| 15.5 V          | 0.93 A          | 0.32 A | 30.0 V         | 10.2 V | 0.94 A | 0.015 A        |
| \( R_{\text{mp}} \) | \( R_{\text{mb}} \) | \( R_{\text{up}} \) | \( R_{\text{bp}} \) | \( Z_T \) | \( R_J \) | \( V_{\text{GS,mp}} \) |
| 18.25 \( \Omega \) | 49.11 \( \Omega \) | 32 \( \Omega \) | 657 \( \Omega \) | 31.9 \( \Omega \) | 20.1 \( \Omega \) | 0.85 V          |
| \( V_{\text{GS,mb}} \) | \( V_{\text{GS,up}} \) | \( V_{\text{GS,bp}} \) | \( V_{\text{GS,m}} \) | \( V_{\text{GS,b}} \) | \( V_{\text{DD,mp}} \) | \( V_{\text{DD,mb}} \) |
| 2.64 V          | 1.35 V          | 4.20 V | -3.0 V         | -4.4 V | 16.3 V | 33.0 V          |

The combiner circuit connected at the package reference planes as shown in Fig. 2(c) is calculated using (19) to be

\[
S_P(\omega) = \begin{bmatrix}
-0.06 + j0.30 & 0.27 - j0.39 \\
0.27 - j0.39 & -0.69 - j0.10
\end{bmatrix}.
\]  

(23)

Fig. 8(a) presents the incident powers for the main (marked with blue rectangles) and auxiliary (marked with black circles) PAs predicted by the embedding device model in Fig. 2(a). It is noted that the DPA at the package reference planes is directly driven at the gate of the transistors by using the two RF-power ports as indicated in Fig. 2(c) without the input matching networks being added yet. The input phase offsets obtained from (22) are marked by the red triangles in Fig. 8(b). The input phase offsets are varying from a larger angle at...
Fig. 8. (a) Incident power and input phase offset angles versus output power at 2 GHz used in the DPA simulations at the package reference plane. (b) Simulated gain and drain efficiency versus output power at 2 GHz by using the embedding device model and the package device model CGH27015.

Low power to a smaller angle at high power. Similar patterns are also observed from the CW measurements in Section IV. In Fig. 8(b), the drain efficiency and gain predicted by the embedding device model at the package reference plane based on Fig. 2(a) are indicated by blue circles and rectangles, respectively. The simulated drain efficiency and gain using the package device model (Wolfspeed CGH27015) based on Fig. 2(c) are indicated by the red circles and rectangles, respectively. The minor discrepancy shown in Fig. 2(a) is due to the fact that the S-parameters of the two-port combiner used for the package DPA simulation must be modified and deviated from the desired S-parameters that were directly calculated from (20) in order to realize it with reciprocal and lossless passive circuits. The simulated fundamental load modulation behaviors for the main and auxiliary PAs based on the DPA prototype at the current-source reference plane are presented in Fig. 9(a) and (b), respectively. The optimal second and third harmonic impedances at the output package reference planes seen by the main and auxiliary PA are also presented in Fig. 9(a) and (b), respectively.

For single frequency DPA output combiners, there are many design choices. In this work, a traditional combiner topology implemented by transmission lines is adopted as shown in Fig. 10. The parameters of the transmission lines are synthesized by targeting the S-parameters goals from (23) at 2 GHz. Meanwhile, alternative combiner topologies can be found in [16] realized by - or T-networks. The output harmonic filter circuits are designed by offset transmission lines and open stubs to match the harmonic impedance goals indicated in Fig. 9(a) and (b). The input matching networks are also designed. The conjugate matching is applied for the
Fig. 11. Schematic of the proposed dual-input asymmetric DPA demonstrator circuit.

Fig. 12. Schematic of the LSNA testbed used for the DPA CW measurements and the fabricated DPA circuits board.

fundamental input impedances and the input second-harmonic impedances are predicted by the embedding device models and then properly fine-tuned to maximize efficiency and avoid the efficiency null [25]. The \( RC \) network implemented by a 1-pF capacitor and a 100-\( \Omega \) resistor is used to stabilize the DPA circuit.

The 2-GHz dual-input Doherty PA demonstrator board is built on a Duroid 5880 substrate with a relative dielectric constant of 2.2 and a thickness of 31 mil. Two Wolfspeed CGH27015 15-W transistors are used for the fabrication. Fig. 11 shows the DPA schematic and the fabricated DPA is shown in Fig. 12. The main amplifier is biased at 16.5 V for the drain with 58-mA dc quiescent current. The auxiliary amplifier is biased at \(-3.8 \) V for the gate and 33 V for the drain. The measurement results are presented in Section IV.

IV. MEASUREMENT RESULTS

A large-signal network analyzer (LSNA) as shown in Fig. 12 is used for performing CW measurements at 2 GHz. In this work, a classical Doherty load modulation with a 90° input phase difference is realized at the current-source reference plane. Since the nonlinear embedding process is nonreciprocal, lossy, and power dependent, the input phase offset angles at the package reference plane will need to depart from 90° as determined from (22). Thereby, the Doherty dual-input RF ports are driven by two phase-locked signal-source generators (Keysight ESG 4438C) and the phase difference between the dual-input

Fig. 13. (a) Measured PAE and gain compared with simulated PAE and gain at 2 GHz. (b) Measured optimal efficiency, gain, and input phase offset angles versus output power at 2 GHz.
is swept from approximately from 70° to 100°. The incident and reflected powers of the main PA at ports 1 and auxiliary PA at ports 2 are measured using two external directional couplers as indicated in Fig. 12, respectively. The output power data are acquired with a power meter (HP 438B) and the dc currents are recorded by the two dc supplies. With different input phase offset angles applied, a variety of CW measurement results are plotted and compared with the Keysight ADS EM Co-simulation data in Fig. 13(a). The discrepancy between the measured power-added efficiency (PAE) and the simulated PAE was verified with the LSNA and originated from the inaccuracy of the model when the transistor is biased at class-C operation.

Fig. 13(b) shows the optimal measured PAE envelope versus output power extracted from Fig. 13(a). The measured associated input phase offsets, drain efficiency, and gain are also indicated in Fig. 13(b). A 65% measured drain efficiency and 62% measured PAE are achieved at 8-dB backoff power with a peak power of about 42.9 dBm and a measured saturation gain of about 15 dB. It is noted that in this work, the dual-input gain (in decibel) is calculated using the difference between the output power and the combined input power added from the two RF input ports.

The fabricated DPA has also been evaluated with both 10- and 20-MHz local thermal equilibrium (LTE) signals exhibiting 9.6- and 9.55-dB PAPR, respectively. The linearization method adopted in this paper is the same as in [24]. A lookup table (LUT) is created based on the CW measurement results as shown in Fig. 13(b). This LUT includes the PA output power as a function of the dual incident powers and the input phase offset. Next, an inverse PA model is implemented using the generalized cubic-spline basis [35]. The predistorted waveforms are then generated using this inverse PA model. It is worth mentioning that for demonstration purpose, the same waveforms were used for both the inverse model extraction and the linearization. When the DPA is excited with a 10-MHz LTE signal, 51.4% of average PAE and around −49.8-dBc adjacent channel leakage ratio (ACLR) are achieved at an average output power of 33.8 dBm after applying DPD. When the DPA is excited with 20-MHz LTE signal, 51.6% of average PAE and around −47.1 dBc of ACLR are achieved at an average output power of 33.8 dBm after applying DPD. The modulated signal measurements are also summarized in Table II. The spectral density before and after applying DPD for 10- and 20-MHz LTE signals is shown in Fig. 14(a) and (b), respectively. The AM/AM and AM/PM before and after applying DPD for (a) 10-MHz and (b) 20-MHz LTE signals at 2 GHz.
10- and 20-MHz LTE signals are shown in Fig. 15(a) and (b), respectively. In Table III, the performance of the Doherty PA in this paper is compared with other recent works found in the literature reviews.

V. CONCLUSION

A novel generalized Doherty PA theory has been developed that results in a direct Doherty PA design methodology targeting high performances. The analysis is first performed at the current-source reference planes for a Doherty PA prototype with a noninfinitly backoff impedance seen by the auxiliary PA at the current-source reference planes is established. The Doherty output combiner that sustains the desired PA performances at the package reference plane is then predicted using the embedding device models. Based on the Doherty PA theory proposed in this work, a software program using ADS-MATLAB cosimulations has been implemented to facilitate the Doherty PA prototype design in less than 24 s. The software program developed in this work accelerates the design of Doherty PAs and allows the PA designer to explore the design space to obtain a DPA with the desired gain-linearity-efficiency tradeoff. The theory and the software program were then used to design a Doherty PA demonstrator operating at 2 GHz. The fabricated Doherty PA demonstrator circuit was evaluated using CW measurements and modulated signal measurements to validate the theory and demonstrate the efficacy of the automatic design tool reported in this paper.

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