Class-E PA Prototype Using An Embedding Model
Invited Paper

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Abstract—This paper reviews the accelerated design of power amplifiers (PA) using a nonlinear embedding device model. Examples of practical application to the design Class F, continuous Class-J and Chireix PAs are presented together with the use of a graphic interface (GUI) for the automatic design of dual-input Doherty PAs. Preliminary simulation results on the application of nonlinear embedding to the design of PAs operating in class E at the current-source reference planes are also reported. A modified embedding device model is used for this purpose.

Keywords—Class-E, power amplifier, nonlinear embedding.

I. INTRODUCTION
The current techniques used for designing for RF power amplifiers (PA) are tedious and time consuming. In this paper a technique for the accelerated design of RF PAs using a nonlinear embedding device model is reviewed [1]. The use of a nonlinear embedding accelerates the design of PAs that are targeted to operate in a specific desired class at the current-source reference planes [2]. When using model-based embedding, this is done by determining, in a single simulation, the source and load impedance terminations required at the package reference planes to sustain the desired intrinsic operation.

In the first part of this paper, examples of single transistor PAs designed using embedding such as class F and broadband class J are first briefly reviewed. The design of dual-input PAs such as Doherty, and Chireix PAs is also presented. An interactive GUI for the automatic design of dual-input Doherty PA prototype at the package reference planes is also briefly discussed.

In the second part of this paper, the design of a prototype class-E PA using model based nonlinear embedding is investigated in simulation at both the current-source and package reference planes.

A. The Nonlinear Embedding Model
Before introducing the embedding model let us first consider the conventional model shown in Fig. 1(a). This model is partitioned in two blocks: (1) the IV characteristics (red FET symbol) and (2) the nonlinear charges and linear parasitics surrounding it (black box). The embedding model shown in Fig. 1(b) also features two similar partitions. However, while the normal model is driven by applying voltages at the package reference planes, the embedding model circuit is driven by applying voltages directly to IV characteristic block. The purpose of the top block in Fig. 1(b) is to provide the voltages and currents at the package reference planes which are required to sustain the device operation at the current-source reference planes.

By providing both voltages and currents at the package reference planes, the nonlinear embedding model eliminates the need for performing source-pull and load-pull simulations at the package reference planes. As we will see in the next section that the embedding model yields the optimal source and load impedance terminations in a single and rapid simulation for each power level and bias.

B. Application to Class F and J
The embedding model facilitates the design of class F PAs at the current-source reference planes. In Class F, the odd harmonics and the even harmonics at the drain current-source reference planes must be terminated by open and short circuits respectively. This permits the formation of quasi-rectangular drain-to-source voltage waveform $v_{DS}$ as shown in Fig. 2 while the drain current is approximately a half-rectified sinusoidal such that the instantaneous $i_D \times v_{DS}$ remain nearly null.

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Applying these impedance boundary conditions to the IV characteristics, the embedding model predicts then the location of all the harmonic impedance termination at the package reference planes in a single simulation. The 3rd harmonic load impedance termination predicted by the embedding model at the package reference planes is shown in Fig. 3 (red circle and cross). The contour plot for a 3rd harmonic load-pull measurement is also reported in Fig. 3 and found to yield the same optimal 3rd harmonic impedance termination as the embedding model.

![Figure 3 Third harmonic load-pull for a class F PA.](image)

Continuous class J PA can also be developed with the help of the embedding device model to more rapidly develop broadband PAs. The drain efficiency, output power and power gain of a continuous class J PA developed using the embedding model [3] are shown in Fig. 4. A demonstrator PA was designed which maintains 60 to 70% efficiency from 1.3 to 2.4 GHz while providing 40 dBm output power.

![Figure 4 Drain efficiency, output power and gain of a class-J PA.](image)

Chireix PA can also be readily developed using the embedding model. The load lines and load impedances before and after embedding are shown in Fig. 5(a) and (b) respectively. Analytic equations in terms of the optimal load and PAPR have been provided for the design of Chireix PA in [4]. An outphasing demonstrator PA designed using nonlinear embedding was reported in [4]. The resulting efficiency versus output power is shown in Fig. 6. The PA delivered 44 dBm peak power at 1.9 GHz with 59.4% average efficiency for 10 MHz LTE with 9.6 dB PAPR.

![Figure 5 Loadlines and load impedance at the current-source and package reference planes of a Chireix PA.](image)

![Figure 6 Drain efficiency and gain of the demonstrator Chireix PA versus its output power for different outphasing angles.](image)

The accelerated design of multi-transistor Doherty PAs can be similarly performed using a nonlinear embedding model [5]. A MATLAB/ADS software tool for the automatic design of Doherty PAs was recently reported [6]. This tool was publicly demonstrated in the 2019 RWW Demo Track with the design of a Doherty PA in 15 s at the package reference planes. In the GUI of this tool in Fig. 7, the user specifies the center frequency, maximum drain current, maximum drain voltage and the desired peak-to-average power ratio (PAPR) setting the DPA asymmetry. Benefiting from the improved convergence of the embedding model, the performance of the designed Doherty PA is then verified for 30 different input power levels in 25 s using harmonic balance simulations using the embedding device model.

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Using this tool, it is possible to explore the tradeoff between gain and efficiency in a Doherty PA. This reported in Fig. 8 using the design parameter \( n_{ap} \) introduced in [6].

**Figure 8** Gain and efficiency of a Doherty PA versus the \( n_{ap} \) factor.

II. CLASS-E PA PROTOTYPE

A. Modified Embedding Model

In this rest of this paper the use of a nonlinear embedding model to design of Class-E PA prototype is investigated. When designing using an embedding model a PA operating in class F, F’1, B, B’1 or C at the current-source reference planes, the fundamental load impedance termination is resistive and it is sufficient to use the IV characteristics to design the PA. However, as is shown in Fig. 9, in a class-E PA a capacitor between drain and source is required to establish the desired mode of operation. The original goal in this effort was to rely solely on the nonlinear drain-to-source capacitance provided by the device. This drain-to-source capacitance is contributed by both the drain-to-gate and the drain-to-source nonlinear charges as shown in Fig. 10(a) and in the equations below:

\[
i_D = I_D(v_{GS}, v_{DS}) + i_{DG}(v_{GS}, v_{DS}) + i_{DS}(v_{GS}, v_{DS}),
\]

with \( i_{DG} = \frac{dQ_{DG}(v_{GS}, v_{DS})}{dt} \) & \( i_{DS} = \frac{dQ_{DS}(v_{GS}, v_{DS})}{dt} \).

However, the device drain-to-source capacitance is highly nonlinear and a more robust class-E PA design is obtained if we add an on-wafer capacitance \( C_E \) connected between drain and source. A capacitance of 2 pF is used in this preliminary simulation work. It was verified that this capacitance convey about 90% of the drain displacement current. The frequency of operation was set to 1 GHz to compensate for the capacitance increase and still obtain reasonable output power given the drain voltage swing is inversely proportional to \( C_E \).

Figure 9 Class-E PA implemented with the embedding device model.

The modified partitioning used in this work for both the normal and embedding models is shown in Fig. 10 (a) and (b) respectively. Using the same modified embedding model, it was recently demonstrated in [7] that the required third harmonic voltage in Class F PAs can actually be generated in a lossless fashion by an inductor terminating the lossless displacement currents sustained by the nonlinear drain-to-source and gate-to-drain capacitances. The device IV characteristics is itself operated in such a fashion that it provides an open for the third harmonic (no third harmonic current).

**Figure 10** Normal and embedding models used for the Class-E PA.

B. Simulation Results for a Class-E PA

The circuit used for the class-E PA is shown in Fig. 9. The gate is biased at threshold using a gate voltage \( V_{GS,DC} \) so that the minimum voltage is -4 V. A positive pulse waveform of 4 V is applied to the gate to turn on the device during the desired time window. The resulting gate voltage waveforms are shown in Fig. 11.

**Figure 11** Gate voltage at the current-source and extrinsic ref. planes.
In Fig. 9, the drain terminal is driven by both DC and AC current sources providing a total drain current $i_D$ of the form:

$$i_D(t) = I_{D,DC} + i_{D,RF}$$

with $i_{D,RF} = I_{D1} \cos(\omega t - \phi_0)$. The gate pulse is started at time $t=0$ and the phase $\phi_0$ is selected such that the total current $I_{DE}$ in Fig. 12(a) is zero for $\omega t=0$ and $\omega t=2\phi_0$. It results that the DC drain current is set to be:

$$I_{D,DC} = -I_{D1} \cos \phi_0.$$  

$$PW = DR \frac{\phi_0}{\pi} T_{RF},$$

where $T_{RF}$ is the RF period, $\frac{\phi_0}{\pi}$ the fraction of the RF period the current $i_{DE}$ is positive and $DR$ the duty rate for the fraction of time the transistor is on when the current $i_{DE}$ is positive. The duty rate $DR$ is selected to be 50% in this initial simulation yielding a $PW$ of 224.7 ps. A rise time and fall time of 28 ps is included as part of the pulse duration $PW$. In our simulations an angle of 101.1° was determined using the simulator tuning function to yield the most optimal class-E operation with the resulting drain-to-source voltage waveform shown in Fig. 12(b) nearly zero when the transistor is on. The IV drain current $I_D$ (red), the total capacitance current $i_C$ (blue), and the total drain current $i_{DE}$ (green) are shown in Fig. 12(a). The instantaneous power dissipation is shown in Fig. 12(c). It is seen that the peak positive power dissipation takes place when the capacitor is discharged from 0 to 0.25 ns. When the total current $i_{DE}$ becomes negative from 0.55 to 1 ns, the power dissipation becomes negative and the external capacitance $C_E$ and the drain-to-source capacitances of the transistor release their stored energy to the load. The drain efficiency for this class-E PA is of 98 % with 2.1 W generated at the current-source reference planes (see Table I). At the package reference planes the efficiency and the power are reduced to 91 % and 1.94 W respectively.

<table>
<thead>
<tr>
<th>I_D1</th>
<th>$\eta_1$</th>
<th>PRF</th>
<th>$\eta_{ext}$</th>
<th>PRF_{ext}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.50</td>
<td>98.03</td>
<td>2.08</td>
<td>91.22</td>
<td>1.94</td>
</tr>
</tbody>
</table>

The loadline shown in red in Fig. 13 for the transistor IV indicates that the transistor operation is close to an ideal switch. For the intrinsic mode of operation to be realizable, the load impedance terminations at the on-wafer reference planes (extrinsic) must be located inside the Smith Chart. This is verified to be the case in Fig. 14 for the first 5 harmonics.
We have verified that a class-E operation could be established. However, the projected gate voltage required on-wafer (purple line) in Fig. 11 exhibits strong oscillatory shape indicating that generating such a precise voltage would be difficult. This originates from the use of a pulsed gate voltage waveform at the gate current-source reference plane exhibiting large slope discontinuities. To reduce the impact of these slope discontinuities, the gate pulsed waveform is first sent to a lowpass butterworth filter with a 3 dB pass and stop frequencies of 3.5 and 12.25 times the fundamental frequency (1 GHz) respectively. The resulting pulsed gate waveforms at the current-source and on-wafer reference planes (for 9 different $I_D$) are shown in Fig. 15. The realization of these waveforms becomes now possible.

Using this band-limited gave waveform we now simulate the performance of a class-E PA for 9 different total current amplitude $I_D$ varying from 0.1 to 0.9 A. In these simulations an angle of $102.3^\circ$ was determined using the simulator tuning function to yield the most optimal class-E operation with the resulting drain-to-source voltage waveform shown in Fig. 16(b) nearly zero when the transistor is on. The IV drain current $I_D$ (red), the total capacitance current $i_C$ (blue), and the total current $i_{DE}$ (green) are shown in Fig. 16(a). The instantaneous power dissipation is shown in Fig. 17(c). The loadline shown in red in Fig. 17 for the transistor IV indicates that the transistor operates close to an ideal switch for all the RF currents $I_D$. 

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**Figure 14** Location of the first five harmonic loads $\Gamma_{1(n\omega)}$.  

**Figure 15** Band-limited pulsed gate waveform at the current-source (red) and on-wafer (purple) reference planes respectively.  

**Figure 16** Currents, voltage and dissipated power for all nine $I_D$.  

**Figure 17** Loadlines for $I_D$ and $i_{DE}$ for all nine $I_D$.  

The 2nd–4th harmonic load impedance terminations at the on-wafer extrinsic reference planes are verified in Fig. 18 to all move toward the edge of the Smith Chart when $I_{D1}$ reach 0.9 A.

At the current-source reference planes the drain efficiency for this class-E PA is seen in Table II to vary from 93.9% to 95.2% while the power is varying from 60 mW to 6W. At the on-wafer extrinsic reference planes, the drain efficiency is varying from 82.5% to 88.6% while the power varies from 52 mW to 5.5 W.

### Table II  Drain Efficiency and RF Power for nine $I_{D1}$.

<table>
<thead>
<tr>
<th>$I_{D1}$</th>
<th>$\eta_1$ (%)</th>
<th>$P_{RF}$ (W)</th>
<th>$\eta_{ext}$ (%)</th>
<th>$P_{RF_{ext}}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.10</td>
<td>93.87</td>
<td>0.06</td>
<td>82.54</td>
<td>0.05</td>
</tr>
<tr>
<td>0.20</td>
<td>94.23</td>
<td>0.24</td>
<td>85.10</td>
<td>0.22</td>
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<tr>
<td>0.30</td>
<td>94.52</td>
<td>0.56</td>
<td>86.19</td>
<td>0.52</td>
</tr>
<tr>
<td>0.40</td>
<td>94.75</td>
<td>1.03</td>
<td>86.89</td>
<td>0.95</td>
</tr>
<tr>
<td>0.50</td>
<td>94.93</td>
<td>1.65</td>
<td>87.41</td>
<td>1.52</td>
</tr>
<tr>
<td>0.60</td>
<td>95.06</td>
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<td>87.81</td>
<td>2.26</td>
</tr>
<tr>
<td>0.70</td>
<td>95.15</td>
<td>3.40</td>
<td>88.13</td>
<td>3.16</td>
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<tr>
<td>0.80</td>
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<td>4.56</td>
<td>88.37</td>
<td>4.25</td>
</tr>
<tr>
<td>0.90</td>
<td>95.17</td>
<td>5.93</td>
<td>88.56</td>
<td>5.54</td>
</tr>
</tbody>
</table>

**III. Conclusion**

In this paper preliminary simulation results on the application of the nonlinear embedding model to the design of class-E PAs are presented. A modified topology for the embedding device model was used to account for the device capacitance. In this work it was found necessary to add an intrinsic shunt capacitance to obtain a robust simulation of class-E PAs. Furthermore, it was also found necessary to use a band-limited pulsed gate voltage waveform at package reference planes to obtain realizable on-wafer gate drives. This work suggests that the implementation of PAs operating in class-E at the current-source reference planes is most likely to be realized for on-wafer devices in a RFIC design than with packaged devices.

**Acknowledgments**

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**References**


