Abstract—This paper presents a two-way hybrid Doherty-outphasing power amplifier (HD-OPA) with an optimal efficiency. The HD-OPA consists of a main PA operating in class-F and an auxiliary PA operating in class-C which jointly operate in the Doherty mode at lower power and the outphasing mode at higher power. The peak to backoff fundamental drain voltage ratio of the auxiliary PA is optimized such that the main and auxiliary transistors both deliver their maximum power at peak power. As a result, the outphasing angles between the two inputs need to be changed dynamically with the dual-input power level. This concept is validated by a fabricated 2.08 GHz PA demonstrator circuit with a drain efficiency of 71.1 % at 8 dB backoff power and a drain efficiency of 74.6 % at 45.1 dBm peak power in continuous-wave measurements. When excited with a 20-MHz LTE signal with 9.55 dB peak-to-average-power-ratio, the HD-OPA yields an average efficiency of 56.7 %, average power-added-efficiency of 52.3 % and adjacent-channel-leakage-ratio of -49.0 dBc after linearization.

Index Terms—Doherty-outphasing, dual-input power amplifiers, GaN, non-linear embedding.

I. INTRODUCTION

Doherty-outphasing power amplifiers (PA) have started to draw attentions from PA designers recently, due to their enhanced average efficiency, extended output power back-off range and wider bandwidth. In [1], a wide band dual-input Doherty-outphasing PA topology is determined and implemented based on the Doherty-outphasing continuum theory. Another topology of dual-input Doherty-outphasing PA implemented with four transistors is proposed in [2], where the PA operates as a Doherty PA in the higher power region and a mixed-mode outphasing PA in the lower power region to provide a high average efficiency over an extended power backoff. In [3], a single-input Doherty-Chireix PA is developed. This single-input PA operates like a Doherty PA at lower power by turning off one transistor and operates like a Chireix outphasing PA at higher power using nonlinear source-pulling. In one recent work [4], a generalized analytic Doherty-Chireix continuum has been established based on four fundamental current- and voltage-ratio coefficients: $K_{im} = |I_{mp}|/|I_{mb}|$, $K_{ia} = |I_{ap}|/|I_{ab}|$, $K_{vm} = |V_{mp}|/|V_{mb}|$ and $K_{va} = |V_{ap}|/|V_{ab}|$. The subscript $m$ and $a$ refers to the main and auxiliary PA, respectively. The subscript $p$ and $b$ refers to the peak and backoff power, respectively.

A new type of hybrid Chireix-Doherty PA is uncovered in [4] by setting $K_{vm} = K_{va} = 1$, $K_{ia} \approx \infty$ and $K_{im} = (OBO + 1)/2$, where OBO refers to the output power backoff range. However, the numerical analysis in Section III of [4] reveals that the dual-input PA achieves a better efficiency and higher maximum output power when $K_{va} = OBO/(OBO - 2)$ such that the main and auxiliary transistors can deliver the same power at peak power level. This work reports on the first experimental investigation of the HD-OPA.

This paper is organized as follows. In Section II, a Doherty-Outphasing combiner theory is developed at the current source reference planes. In Section III, the impact of the factor $K_{va}$ is investigated by performing multiple harmonic balance simulations using embedding device models. The optimal $K_{va}$ is selected accordingly to design a dual-input PA demonstrator circuits at the device package reference planes. The experimental verification is presented in Section IV.

Fig. 1 shows the conceptual diagram of the two-way hybrid Doherty-Outphasing PA at the current-source reference planes.

II. DOHERTY-OUTPHASING COMBINER THEORY

Fig. 1 shows the conceptual diagram of the two-way hybrid Doherty-Outphasing PA at the current-source reference planes. Two devices (main and auxiliary) are represented by ideal current sources connected by a two-port lossy and reciprocal combiner network. This two-port combiner is realized with a lossless and reciprocal three-port combiner terminated with a resistive load $R_L$. As shown in Fig. 1, the impedances seen by the main and auxiliary PA are assumed to
be real \((R_m \text{ and } R_a)\). The \(Z\) parameters of the two-port combiner \(Z\) is given in [4].

In [4], the \(K_{ia}\) for the auxiliary transistor could take any value. In this work, it is assumed that 1) the auxiliary PA is fully turned off at backoff power, which results in \(K_{ia} = \infty\) or sufficiently large and 2) the fundamental voltage of the main PA remains constant from backoff to peak power to achieve high backoff efficiency, which leads to \(K_{vm} = 1\). It results that the OBO in terms of \(K_{im}\) and \(K_{va}\) is derived to be:

\[
OBO = \frac{P_{ap} + P_{mp}}{P_{ab} + P_{mb}} = K_{im} + K_{im}K_{va} - K_{va}. \tag{1}
\]

The asymmetry fundamental peak power ratio \(n\) between the main and auxiliary PAs is given by:

\[
n = \frac{|V_{ap}| |I_{ap}|}{|V_{mp}| |I_{mp}|} = K_{va} - K_{va} \frac{K_{va} - 1}{OBO + K_{va}}. \tag{2}
\]

The two-port network must satisfy the lossless-ness condition \(R_m^2 \{Z_{12}\} = R \{Z_{11}\} R \{Z_{22}\}\) [4]. The outphasing angles at backoff and peak power can then be expressed in terms of the OBO and \(K_{va}\) parameters:

\[
\theta_b = \pm \cos^{-1} \left( \pm \sqrt{\frac{OBO - K_{va}^2}{OBO + 2K_{va} + 1}} \right), \quad \theta_p = \pi - \theta_b. \tag{3}
\]

### III. Design and Simulations

HD-OPA prototypes associated with multiple values of \(K_{va}\) running from 1 to 3 are first investigated at the current-source reference planes using the embedding device model introduced in [5]. These harmonic balance simulations are performed automatically using MATLAB-ADS co-simulations [6] and [7]. The HD-OPA prototype is then established by selecting the optimized value of \(K_{va}\). Finally, a 2.1 GHz HD-OPA demonstrator circuit is realized and fabricated using the projected voltage and current waveforms at the package reference planes.

The PA simulations are performed based on the schematic shown in Fig. 1. The values of \(K_{im}\) are calculated from (1) after setting OBO = 9 and sweeping \(K_{va}\) from 1 to 3 with a step of 0.1. In this work, the maximum fundamental drain voltages for the main \(|V_{mp}|\) and auxiliary PAs \(|V_{ap}|\) are both set to 24 V. The maximum fundamental auxiliary drain current of \(|I_{ap}| = 1.0\) A is selected, which corresponds to a maximum instantaneous device current of 2 A \((I_{\text{max}} \approx 2\) A). The maximum fundamental drain currents for main PA \(|I_{mp}|\) are then obtained from (2). The outphasing angles \(\theta_b\) are given by (3) and the \(Z\) parameters of the two-port output combiners at the current-source reference planes are obtained from [4]. The input-RF voltage drives \(V_{GS,m/a}\) for main and auxiliary PA are swept and extracted from the numerical interpolation based on the simulation test bench presented in Fig. 2, where the embedding device models are terminated with the resistors \(R_{m/ap}\) at backoff or \(R_{m/ab}\) at peak power. The intrinsic harmonic are properly terminated to create class-F operation for the main PA, and class-C operation for the auxiliary PA. The simulated drain efficiency (blue curves) and gain (cyan curves) in Fig. 3 are plotted versus output power as \(K_{va}\) increases from
1 to 3. The simulated drain efficiency of the HD-OPA prototypes (highlighted in black) obtained with $K_{va} = 1.3$ is significantly higher than that of Doherty PA prototype (highlighted in red) when $K_{va} = 3$ without compromising the gain. Meanwhile, the efficiency using $K_{va} = 1.3$ is also better than the one proposed in [4] for the HCD-PA, where $K_{va} = 1$ (highlighted in purple). Furthermore, it is seen that the gain becomes more linear and the maximum output power becomes higher than the HCD-PA by 0.46 dB and higher than the Doherty PA by 1.25 dB for the same OBO of 9.54 dB [4]. Fig. 4 shows the load modulation trajectories with different values of $K_{va}$. The modulated load seen by the HD-OPA become complex as the output power increases, which is distinctive from the purely real impedances exhibited by the Doherty PA.

Based on the above simulations, $K_{va} = 1.3$ is the optimal choice for the HD-OPA design. It is worth mentioning that the simulated $K_{va} = 1.3$ is close to the theoretical solution of $K_{va} = \text{OBO}/(\text{OBO}−2) = 1.28$ obtained from (2) with OBO = 9 for 9.54 dB backoff range and $n = 1$ for a symmetric peak power ratio between the main and auxiliary devices. The outphasing angles based on (3) are $\theta_b = 40.4^\circ$ and $\theta_p = 139.6^\circ$, respectively. The $S$-parameters of the output combiner at the package reference planes which are extracted by absorbing the linear and non-linear parasitics at 2.1 GHz using the nonlinear embedding technique [5], are given by:

$$S_P(\omega) = \begin{bmatrix} -0.35 - j0.64 & -0.51 + j0.13 \\ -0.51 + j0.13 & 0.07 - j0.02 \end{bmatrix}.$$ 

The output combiner circuits are then synthesized, optimized and implemented using transmission lines as shown in Fig. 5. The PA demonstrator circuit also shown in Fig. 5 is built on a Rogers Duroid 5880 substrate with a $\epsilon_r = 2.1$ and thickness of 31 mils. Two Wolfspeed CGH40010 GaN transistors are used for this implementation. The same drain bias of 25 V is used for the two transistors. The DC quiescent current for the main PA is 60 mA and the gate bias for the main and auxiliary PA are -2.54 V and -4.1 V, respectively. The measurement results are presented in the next section.

**IV. EXPERIMENTAL VERIFICATION**

It has been found that the best efficiency was achieved at 2.08 GHz due to a 20 MHz frequency shift after the PA fabrication. Fig. 6 shows that the simulated data obtained from the ADS simulations are comparable to the continuous-wave (CW) measured data acquired using a non-linear vector network analyzer (NVNA). The measured optimal drain efficiency (in black circles) of 71.1 % at 8 dB backoff and 74.6 % at the peak power of 32.5 W are achieved using the NVNA as shown in Fig. 6. The optimal outphasing angles used indicated by the purple triangles are also shown in Fig. 6. The related optimal gain as indicated by the black circles in Fig. 7 is

### TABLE I
Measurement Results with 20 MHz LTE Signals.

<table>
<thead>
<tr>
<th>DPD</th>
<th>Input PAPR (dB)</th>
<th>$P_{\text{out-avg}}$ (dBm)</th>
<th>$\text{DE}_{\text{avg}}$ (%)</th>
<th>Gain (dB)</th>
<th>$\text{ACLR}$ (dBc)</th>
<th>$\text{NMSE}$ (dB)</th>
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</thead>
<tbody>
<tr>
<td>Before</td>
<td>9.55</td>
<td>35.5</td>
<td>57.0 / 52.8</td>
<td>11.3</td>
<td>-30.7</td>
<td>-20.7</td>
</tr>
<tr>
<td>After</td>
<td>9.55</td>
<td>35.5</td>
<td>56.7 / 52.3</td>
<td>11.4</td>
<td>-49.0</td>
<td>-34.6</td>
</tr>
<tr>
<td>Before</td>
<td>7.0</td>
<td>38.0</td>
<td>63.6 / 59.2</td>
<td>11.5</td>
<td>-27.8</td>
<td>-20.3</td>
</tr>
<tr>
<td>After</td>
<td>7.0</td>
<td>37.6</td>
<td>62.9 / 58.1</td>
<td>11.3</td>
<td>-49.7</td>
<td>-25.7</td>
</tr>
</tbody>
</table>

Fig. 6. Measured drain efficiency and outphasing angles of the HD-OPA at 2.08 GHz.

Fig. 7. Measured gain of the HD-OPA at 2.08 GHz.
above 10.0 dB across the entire output power range with a variation of less than 2 dB. The dual-input gain in this work is defined as the ratio between the output power and the sum of the incident power of both input ports. It is to be noted that the optimal outphasing angle selected in Fig. 6 is not always yielding the highest efficiency envelope, since it is also necessary to maintain a relatively linear gain in Fig. 7. The PA is also tested from 2.05 GHz to 2.1 GHz as shown in Fig. 8. The dynamic response of the HD-OPA was verified with 20 MHz input LTE signals exhibiting 9.55 dB and 7.0 dB peak-to-average power ratio (PAPR). The same digital pre-distortion (DPD) linearization technique is applied as reported in [8]. The measured data using these LTE signals are summarized in Table I. Table II compares the HD-OPA in this paper with other dual-input PAs recently reported in the literature. The output power spectra density (PSD) of this PA before and after linearization are shown in Fig. 9.

### TABLE II
Comparison of the Recent State-of-the-art Dual-Input Power Amplifiers.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Frequency (GHz)</th>
<th>Instant. BW (MHz)</th>
<th>DEavg/PAE (%)</th>
<th>PAPR (dB)</th>
<th>ACLR (dBc)</th>
<th>Reference</th>
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</thead>
<tbody>
<tr>
<td>GaN</td>
<td>1.2-3.7</td>
<td>-</td>
<td>40</td>
<td>6.7</td>
<td>-58</td>
<td>[1]</td>
</tr>
<tr>
<td>GaN</td>
<td>2.14</td>
<td>-</td>
<td>-</td>
<td>36.0</td>
<td>-32</td>
<td>[2]</td>
</tr>
<tr>
<td>LDMOS</td>
<td>2.17</td>
<td>3.84</td>
<td>45/43.4</td>
<td>7.5</td>
<td>-56.2</td>
<td>[3]</td>
</tr>
<tr>
<td>GaN</td>
<td>0.58</td>
<td>10</td>
<td>70/20</td>
<td>10.4</td>
<td>-47.7</td>
<td>[4]</td>
</tr>
<tr>
<td>GaN</td>
<td>1.4-4.8</td>
<td>-</td>
<td>43/40</td>
<td>6.0</td>
<td>-</td>
<td>[10]</td>
</tr>
<tr>
<td>GaN</td>
<td>2.08</td>
<td>20</td>
<td>56/75/23</td>
<td>9.55</td>
<td>-49</td>
<td>This work</td>
</tr>
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</table>

**V. Conclusion**

This work reports on the first experimental investigation of the optimal hybrid Doherty-outphasing PA. The existence of an optimal design choice for the peak-to-backoff voltage ratio for the auxiliary PA, which maximizes both efficiency and peak power while maintaining an acceptable linearity, was first demonstrated. A 2.08 GHz dual-input demonstrator PA circuit was then implemented and experimentally tested to validate the theory.

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**REFERENCES**


