Asymmetrically-Driven Current-Based Chireix Class-F Power Amplifier Designed using an Embedding Device Model

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Abstract—Model-based nonlinear embedding is applied for the first time to the design of an asymmetrically-driven class-F Chireix power amplifier (PA). The embedding model of a 15 W GaN HEMT is used to determine the optimum load impedances for the fundamental and multi-harmonics required at the package reference planes such that the two intrinsic transistors operate with a recently reported ideal current-based Chireix combiner. A symmetric circuit topology is used so that the phase offset of the Chireix combiner is maintained throughout the design from the intrinsic and packaged nodes up to the drive generators. Unlike the conventional Chireix PA, which is driven with constant envelope signals, this PA designed using embedding is found to require asymmetrical amplitude and phase modulated input drives to support the targeted equal-power input signals at the intrinsic reference planes. The Chireix PA designed exhibits a peak drain efficiency of 79.6 % and power added-efficiency (PAE) over 77/71% around peak power (43/44 dBm) and 55% at 8dB backoff power (36dBm) at 2 GHz as measured with a large-signal network analyzer (LSNA). Using a lookup table driver, the PA average drain efficiency is 50% for a 5 MHz W-CDMA signal with 9.3 dB PAPR and -41.5 dBc ACPR achieved.

Index Terms—Chireix, outphasing, power amplifiers

I. INTRODUCTION

The Chireix outphasing architecture is one of the most intriguing techniques for designing high efficiency RF PAs. The original Chireix outphasing architecture consists of two amplifiers and one lossless combiner typically implemented using a stub and one quarter wave transmission line in each path [1]. According to the Chireix combiner theory [1], the two amplifiers can then be both operated in saturation with constant envelope signals using only phase modulation to ensure a high efficiency operation for a wide range of output power.

Conventional Chireix combiner theory is usually presented using ideal voltage sources for the transistors and thus neglects the linear and nonlinear device parasitics between the intrinsic and the packaged reference planes of both transistors [2]. Load-pull technique can then be used to search for the load which compensates for the linear and nonlinear device parasitics such that PAs operate with outphasing [3].

Unlike the conventional Chireix theory, this work relies on a novel current-based Chireix outphasing analysis [4] used in conjunction with a nonlinear embedding model [5]. The embedding device model provides direct access to the intrinsic current source of the transistor. By directly designing an ideal Chireix PA with the intrinsic transistor IVs, one can directly set the desired intrinsic drain load values without using a load-pull search technique at the package reference planes. Analysis with the nonlinear embedding model enables then to design the Chireix PA like if the intrinsic devices (IV) were directly connected to the Chireix current combiner while simultaneously establishing the extrinsic loads which yields this desired ideal intrinsic Chireix outphasing operation. Using this exact embedding approach it is found that asymmetric input signal drives are required at the package reference plane to sustain the targeted ideal Chireix operation mode at the intrinsic reference planes.

II. CURRENT-BASED CHIREIX PA DESIGN USING AN EMBEDDING DEVICE MODEL

Fig. 1 shows a symbolic representation of (a) the device model and (b) the non-linear embedding model for a GaN HEMT with the FET intrinsic IV shown in red. The embedding device model generates the required voltages and currents at the package reference planes when an ideal virtual circuit is implemented with the FET intrinsic IV (red).

Fig. 2 shows the initial intrinsic design using the embedding model associated with lossless class-F harmonic terminations and lossless Chireix combiner. Note that the lossless network shown above are all “virtual” in this initial design stage.
However the final circuit designed will emulate their operation.

The analytic expressions reported in [4] are used for the two lossless 2-port networks such that the transistor operates with real loads $R_{min}$ and $R_{max}$ at peak and backoff, respectively and such that the load currents verify:

$$I_1 = I(\theta)[\cos(\theta) + j \sin(\theta)],$$

$$I_2 = I(\theta)[\cos(\theta) - j \sin(\theta)],$$

$$I_{12} = 2 I(\theta) \cos(\theta).$$

with $\theta$ being the out-phasing angle. The differential phase is $\theta_{diff} = \theta - (-\theta) = 2\theta$. When $\theta = 0$, the maximum power is achieved as the combiner provides the drain current sources with the optimal $R_{min}$. When $\theta = \theta_0$, defined as the outphasing angle of backoff power, the combiner provides the drain current sources with a maximum load $R_{max}$. It results from (3) that the peak-to-average power ratio (PAPR) is set by $\cos^{-2}(\theta_0)$ such that we have:

$$\theta_0 = \cos^{-1}\left(10^{-\frac{PAPR\,(dB)}{20}}\right).$$

Based on the topology shown in Fig. 2 and (4), we can easily set the optimum input intrinsic voltage signal for driving this ideal load at the selected outphasing angle. In our design $\theta$ varies from 0 to 66.54 degree based on the selected 8 dB PAPR with $R_{min} = 26$ Ohm and $R_{max} = 188$ Ohm. Note that the final differential phase $\theta_{diff}$ will slightly depart from the ideal $\theta_{diff}$ because of the non-ideal harmonic terminations and quasi-symmetric Chireix combiner designed.

### III. OUTPHASING CIRCUIT DESIGN

#### A. Exact Asymmetric Package Input Signal Design

In order to streamline the design process while maintaining the optimum intrinsic input signals, the Chireix combiner network is directly extracted from the two critical extreme conditions: peak power ($\theta = 0$) and 8dB backoff power ($\theta = \theta_0$) [4]. For power levels in between backoff and peak, the optimal outphasing angle for each incident power $P_{inc}(\theta)$ is obtained in simulation so that the efficiency is maximized.

Note that the same incident power $P_{inc}(\theta)$ is used for the top and bottom transistors at the intrinsic reference planes.

Having established the optimum input signals, we turn now toward the optimal output loads predicted by the embedding model shown in Fig. 2.

Fig. 4 (a) shows the intrinsic load lines at both peak and 8 dB backoff power. (b) Plot of the reflection coefficients $\Gamma_1(\omega, 2\omega, 3\omega)$ provided by the Chireix combiner at the intrinsic and package reference planes before and after projection with the embedding model respectively.

Fig. 3 (a) shows the asymmetric projected $\Gamma_{IN}(\omega)$ at the package reference planes and (b) the associated required input power for the two (top and bottom) transistors as predicted by the non-linear embedding device model from the targeted linearly varying intrinsic input signals. It is seen that both the projected $\Gamma_{IN}(\omega)$ and the input power are power-dependent throughout the 8dB PAPR output power range. The projected input power $P_{in}(top)$ and $P_{in}(bottom)$ at the package reference planes are also strongly asymmetric throughout the 8dB PAPR output power range. Thus the need for an asymmetric drive for the top and bottom stages at the package reference planes to support the targeted linearly-varying equal-power input signals at the intrinsic reference planes.

#### B. ADS Simulation & Circuit Synthesis

Fig. 4 (a) shows the intrinsic load line at peak and 8 dB backoff power. (b) Plot of the reflection coefficients $\Gamma_1(\omega, 2\omega, 3\omega)$ provided by the Chireix combiner at the intrinsic and package reference planes before and after projection with the embedding model respectively.
nals. The intrinsic harmonic reflection coefficients $\Gamma_{\text{intrinsic}}(2\omega, 3\omega)$ are set to short and open, respectively for class F operation. The embedding model then precisely yields the corresponding ideal $\Gamma_\ell(\omega, 2\omega, 3\omega)$ at the package reference planes. Lossless harmonic terminations can then be easily designed to match the projected $\Gamma_\ell(2\omega, 3\omega)$.

The real harmonic termination is developed using a microstrip line based design with the help of the optimizing tools in ADS. The ABCD matrix is used for transforming the voltage and current signals from the package drain to port 1 & 2 as shown in Fig. 2 across the harmonic termination network. Since the voltage and current signals are given at port 1 & 2, we can readily design a Chireix combiner to meet the quasi-lossless and reciprocal conditions [4]. In summary model-based nonlinear embedding greatly facilitates the Chireix PA design by accounting for the linear and nonlinear parasitics.

IV. CW LSNA & WCDMA DPD MEASUREMENT RESULTS

Fig. 5 shows the schematic of the designed 2 GHz Chireix outphasing PA with 8 dB PAPR. Two 15 W GaN HEMTs (CGH27015F) were used. A quasi-symmetric micro-strip line-based circuit-structure was developed.

Fig. 6 shows the results of two-dimensional power and phase sweep CW measurements with a large signal network analyzer (LSNA). Note that both transistors are driven by the asymmetric input signals established in the ADS emCosim. Since the input matching network is designed for the 8 dB backoff power, the PAE matches precisely with the drain efficiency at backoff. The typical mixed mode optimal efficiency envelope is also shown using a red line in Fig. 6. It exhibits a significant improvement in efficiency at lower powers compared to the traditional pure outphasing mode [2]. The efficiency envelope shown in red in Fig. 6 keeps the PAE over 55% over nearly the full 8 dB PAPR range for this mixed mode operation with a power gain of 11/14 dB.

In Fig. 7, at each power levels, the efficiencies at the selected $\theta_{\text{diff}}$ of LSNA measurement exhibits an excellent agreement with the ADS emCosim. The ADS emCosim simulated full 360 degrees $\theta_{\text{diff}}$ are shown in Fig. 7. For the LSNA measurements, the $\theta_{\text{diff}}$ sweeping range was from -150 to -40 degrees at 8 dB backoff power, yielding around 36 dBm output power with 56% drain efficiency. Figure. 7 shows that $\theta_{\text{diff}}$ obtained from the simulations and measurements are 38.9 and -39.3 degrees, respectively. In order to prevent the GaN transistor to be operated at too high temperatures around 44 dBm peak output power, the $\theta_{\text{diff}}$ sweeping range was decreased to the range -150 to -80 degrees. Figure. 7 also shows that at peak power, the outphasing angle $\theta_{\text{diff}}$ obtained from the simulations and measurements are -137.7 and -140.8 degrees, respectively with nearly the same drain efficiency of 73%.

Fig. 7 Comparison between the drain efficiencies obtained from asymmetric input power CW LSNA measurements and ADS emCosim simulations.

**TABLE I**

<table>
<thead>
<tr>
<th>Device</th>
<th>Architecture</th>
<th>Freq (MHz)</th>
<th>Signal (dBm)</th>
<th>$\eta$ &amp; PAE (Avg)</th>
<th>PAPR</th>
<th>ACPR Peak (W)</th>
<th>Ref</th>
<th>Note</th>
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<td>50.5/47.8</td>
<td>9.6 - 47</td>
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<td>9.55 - 33</td>
<td>110</td>
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<td>9.6 - 45.4</td>
<td>75</td>
<td>[7]</td>
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<tr>
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<td>65.6/65.4</td>
<td>7.5</td>
<td>93</td>
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<td>50.7</td>
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<td>45</td>
<td>30 This work</td>
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Note: OSO co-design with PA at device level, $^*$ with LUT pre-distortion.
Fig. 8 shows the DPD measurement results with a modulated 5 MHz W-CDMA signal. An average drain efficiency of 50% with 9.3 dB PAPR can be achieved using a LUT power and phase driver. An ACPR of -41.5 dB can be achieved after DPD linearization with a slight increase in efficiency.

V. CONCLUSIONS

A novel procedure for designing Chireix PAs is presented in which a virtual Chireix PA is first designed using the intrinsic transistor IVs and a recently reported current-based Chireix combiner. The embedding model then determines the asymmetric input signals and impedances at the package reference planes required to sustain this ideal Chireix intrinsic operation. The Chireix PA achieves 79.6% peak drain efficiency and 71-77% PAE at peak and 55% at 8dB at backoff powers and over 50 % average drain efficiency with a 5 MHz W-CDMA signal at 2 GHz. This design technique can also be used for the design of broadband outphasing PAs.

ACKNOWLEDGMENT

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REFERENCES