Predistortion Linearization TestBed

DUT: Power Amplifier

RF_{out} → PA/DUT → Linear Power Amplifier → IQ Modulator → ADCs → FPGA/DSP → DAC → Interface → Linearization Parameters

Local Oscillator → Spectrum Analyzer

Power Amplifier under test
Altera FPGA/DSP board

<table>
<thead>
<tr>
<th>Feature</th>
<th>EP1S25F780-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic elements (LEs)</td>
<td>25,560</td>
</tr>
<tr>
<td>M512 RAM Blocks (32 × 18 bits)</td>
<td>224</td>
</tr>
<tr>
<td>M4K RAM Blocks (128 × 36 bits)</td>
<td>138</td>
</tr>
<tr>
<td>M-RAM Blocks</td>
<td>2</td>
</tr>
<tr>
<td>Total RAM bits</td>
<td>1,944,576</td>
</tr>
<tr>
<td>DSP Blocks</td>
<td>10</td>
</tr>
<tr>
<td>Embedded multipliers (based on 9 × 9)</td>
<td>80</td>
</tr>
<tr>
<td>PLLs</td>
<td>6</td>
</tr>
<tr>
<td>Maximum user I/O pins</td>
<td>597</td>
</tr>
</tbody>
</table>

- 2 built-in DACs
- 2 built-in ADCs
80 MHz FPGA/DSP Test Bed

External ADC #3

Internal ADCs #1 and #2

DAC to internal IQ mixer Adaptation Stage

DAC to internal IQ mixer Adaptation Stage

External ADC #4

External DAC #3

DAC to external IQ mixer Adaptation Stage

IQ Modulator

DAC to external IQ mixer Adaptation Stage

DAC to internal IQ mixer Adaptation Stage

External DAC #4
FPGA Test-Bed Control using LabWindow

Linearization Control for W-CDMA

Multisine Generator

IMD3 & IMD5 suppression
Preliminary Results for *Memoryless* Predistortion

$I$ and $Q$ for 50 tones multisine

Before linearization

After linearization
Preliminary Results for Memoryless Predistortion

W-CDMA I and Q Signals

Before linearization

After linearization
PA Linearization Targets

• Experimental demonstration of broadband linearization for PAs with memory effects for single & 3-carrier W-CDMA
• Extend new linearization schemes to multi-carrier W-CDMA OFDM/UWB and 4G.