APPENDIX B

TMS320LF2407 PERIPHERAL GUIDE
for
EE757
Control Systems Laboratory

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Engineering

About This Appendix

embedded real-time software applications in EE757 Control Systems Laboratory. The contents of this appendix are taken from the *TMS320C2xx/C24x DSP Controllers Reference Guide for Systems and Peripherals,* and prepared so as to make the students familiar with the tools to be used in EE757 Control Interfacing and Design Laboratory. Its aim is not to serve as a complete guide for the DSP controller, it only covers necessary parts needed in the experiments of EE757. After making a fast introduction to the controller, the reader is encouraged to refer to the guide supplied by *Texas Instruments*

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1 Event Manager (EV)

1.1 EV Pins

Each EV module has eight device pins available for compare/PWM outputs:
Two GP timer compare/PWM output pins:

EVA	EVB
T1CMP/T1PWM	T3CMP/T3PWM
T2CMP/T2PWM	T4CMP/T4PWM

Six (full) compare/PWM output pins:

EVA	EVB
PWM1	PWM7
PWM2	PWM8
PWM3	PWM9
PWM4	PWM10
PWM5	PWM11
PWM6	PWM12

The EVA module uses three device pins, CAP1/QEP1, CAP2/QEP2, and CAP3, as capture or quadrature encoder pulse inputs.
The EVB module uses three device pins, CAP4/QEP3, CAP5/QEP4, and CAP6, as capture or quadrature encoder pulse inputs.
The timers in the EV module can be programmed to operate based on an external clock or the internal device clock. The device pin TCLKINA/B supplies the external clock input. The device pin TDIRA/B is used to specify the counting direction when a GP timer is in directional up-/down-counting mode.

1.2 EV Interrupts

The Event Manager interrupts are arranged into three groups. Each group is assigned one CPU interrupt (INT2, 3 or 4). The interrupt requests are generated as follows:
Interrupt source: If peripheral interrupt conditions occur, the respective flag bits in registers EVxIFRA, EVxIFRB, or EVxIFRC (x = A or B) are set. Once set, these flags remain set until explicity cleared by the software. It is mandatory to clear these flags in the software or future interrupts will not be recognized.
Interrupt enable: The Event Manager interrupts can be individually enabled or disabled by interrupt mask registers EVxIMRA, EVxIMRB, and EVxIMRC (x = A or B). Each bit is set to 1 to enable/unmask the interrupt or cleared to 0 to disable/mask the interrupt.

1.3 General-Purpose (GP) Timers

There are two general-purpose (GP) timers in each module. These timers can be used as independent time bases in applications such as:
- The generation of a sampling period in a control system
- Providing a time base for the operation of the quadrature encoder pulse (QEP) circuit (GP timer 2/4 only) and the capture units
- Providing a time base for the operation of the compare units and

associated PWM circuits to generate PWM outputs

Timer Functional Blocks

Each GP timer includes:

- One readable and writeable (RW) 16-bit up and up/down counter register TxCNT (x = 1, 2, 3, 4). This register stores the current value of the counter and keeps incrementing or decrementing depending on the direction of counting
- One RW 16-bit timer compare register (shadowed), TxCMPR (x = 1, 2, 3, 4)
- One RW 16-bit timer period register (shadowed), TxPR (x = 1, 2, 3, 4)
- RW 16-bit individual timer control register, TxCON (x = 1, 2, 3, 4)
- Programmable prescaler applicable to both internal and external clock inputs
- Control and interrupt logic
- One GP timer compare output pin, TxCMP (x = 1, 2, 3, 4)
- Output conditioning logic

Another overall control register, GPTCONA/B, specifies the action to be taken by the timers on different timer events, and indicates the counting directions of the GP timers. GPTCONA/B is readable and writeable, although writing to the status bits has no effect.

GP Timer Inputs

The inputs to the GP timers are:

- The internal device (CPU) clock
- An external clock, TCLKINA/B, that has a maximum frequency of one-fourth that of the device clock
- Direction input, TDIRA/B, for use by the GP timers in directional up-/down-counting mode
- Reset signal, RESET

When a timer is used with the QEP circuit, the QEP circuit generates both the timer's clock and the counting direction.

GP Timer Outputs

The outputs of the timers are:

- GP timer compare outputs TxCMP, x = 1, 2, 3, 4
- ADC start-of-conversion signal to ADC module
- Underflow, overflow, compare match, and period match signals to its own compare logic and to the compare units
- Counting direction indication bits

Individual GP Timer Control Register (TxCON)

The operational mode of a timer is controlled by its individual control register TxCON. Bits in the TxCON register determine:

- Which of the four counting modes the timer is in
- Whether an internal or external clock is to be used by the GP timer
- Which of the eight input clock prescale factors (ranging from 1 to 1/128) is used
- On which condition the timer compare register is reloaded
- Whether the timer is enabled or disabled
- Whether the timer compare operation is enabled or disabled

- Which period register is used by timer 2, its own, or timer 1's period register (EVA)
- Which period register is used by timer 4, its own, or timer 3's period register (EVB)

Overall GP Timer Control Register (GPTCONA/B)
The control register GPTCONA/B specifies the action to be taken by the timers on different timer events and indicates their counting directions.

GP Timer Compare Registers
The compare register associated with a GP timer stores the value to be constantly compared with the counter of the GP timer. When a match happens, the following events occur:
- A transition occurs on the associated compare output according to the bit pattern in GPTCONA/B
- The corresponding interrupt flag is set
- A peripheral interrupt request is generated if the interrupt is unmasked
- The compare operation of a GP timer can be enabled or disabled by the appropriate bit in TxCON.
The compare operation and outputs can be enabled in any of the timer modes, including QEP mode.

GP Timer Period Register
The value in the period register of a GP timer determines the period of the timer. A GP timer resets to 0, or starts counting downward when a match occurs between the period register and the timer counter, depending on which counting mode the timer is in.

Double Buffering of GP Timer Compare and Period Registers
The compare and period registers, TxCMPR and TxPR, of a GP timer are shadowed. A new value can be written to any of these registers at any time during a period. However, the new value is written to the associated shadow register. For the compare register, the content in the shadow register is loaded into the working (active) register only when a certain timer event specified by TxCON occurs. For the period register, the working register is reloaded with the value in its shadow register only when the value of the counter register TxCNT is 0. The condition on which a compare register is reloaded can be one of the following:
- Immediately after the shadow register is written
- On underflow; that is, when the GP timer counter value is 0
- On underflow or period match; that is, when the counter value is 0 or when the counter value equals the value of the period register.
The double buffering feature of the period and compare registers allows the application code to update the period and compare registers at any time during a period in order to change the timer period and the width of the PWM pulse for the period that follows. On-the-fly change of the timer period value, in the case of PWM generation, means on-the-fly change of PWM carrier frequency.

Caution :

The period register of a GP timer should be initialized before its counter is initialized to a non-zero value. Otherwise, the value of the period register will remain unchanged until the next underflow.

Note that a compare register is transparent (the newly loaded value goes directly into the active register) when the associated compare operation is disabled. This applies to all Event Manager compare registers.

GP Timer Compare Output
The compare output of a GP timer can be specified active high, active low, forced high, or forced low, depending on how the GPTCONA/B bits are configured. It goes from low to high (high to low) on the first compare match when it is active high (low). It then goes from high to low (low to high) on the second compare match if the GP timer is in an up-/down-counting mode, or on period match if the GP timer is in up-counting mode. The timer compare output becomes high (low) right away when it is specified to be forced high (low).

Timer Counting Direction
The counting directions of the GP timers are reflected by their respective bits in GPTCONA/B during all timer operations as follows:
- 1 represents the up-counting direction
- 0 represents the down-counting direction

The input pin TDIRA/B determines the direction of counting when a GP timer is in directional up-/down-counting mode. When TDIRA/B is high, upward counting is specified; when TDIRA/B is low, downward counting is specified.

Timer Clock
The source of the GP timer clock can be the internal device clock or the external clock input, TCLKINA/B. The frequency of the external clock must be less than or equal to one-fourth of that of the device clock. GP timer 2 (EVA) and GP timer 4 (EVB) can be used with the QEP circuits, in directional up-/down-counting mode. In this case, the QEP circuits provide both the clock and direction inputs to the timer.
A wide range of prescale factors are provided for the clock input to each GP timer.

QEP-Based Clock Input
The quadrature encoder pulse (QEP) circuit, when selected, can generate the input clock and counting direction for GP timer 2/4 in the directional up-/down-counting mode. This input clock cannot be scaled by GP timer prescaler circuits (that is, the prescaler of the selected GP timer is always one if the QEP circuit is selected as the clock source). Furthermore, the frequency of the clock generated by the QEP circuits is four times that of the frequency of each QEP input channel because both the rising and falling edges of both QEP input channels are counted by the selected timer. The frequency of the QEP input must be less than or equal to one-fourth of that of the device clock.

Starting the A/D Converter with a Timer Event

The bits in GPTCONA/B can specify that an ADC start signal be generated on a GP timer event such as underflow, compare match, or period match. This feature provides synchronization between the GP timer event and the ADC start without any CPU intervention.

GP Timer Interrupts

There are sixteen interrupt flags in the EVAIFRA, EVAIFRB, EVBIFRA, and EVBIFRB registers for the GP timers. Each of the four GP timers can generate four interrupts upon the following events:

- Overflow: TxOFINT (x = 1, 2, 3, or 4)
- Underflow: TxUFINT (x = 1, 2, 3, or 4)
- Compare match: TxCINT (x = 1, 2, 3, or 4)
- Period match: TxPINT (x = 1, 2, 3, or 4)

A timer compare event (match) happens when the content of a GP timer counter is the same as that of the compare register. The corresponding compare interrupt flag is set one clock cycle after the match if the compare operation is enabled.

An overflow event occurs when the value of the timer counter reaches FFFFh. An underflow event occurs when the timer counter reaches 0000h. Similarly, a period event happens when the value of the timer counter is the same as that of the period register. The overflow, underflow, and period interrupt flags of the timer are set one clock cycle after the occurrence of each individual event.

1.4 GP Timer Counting Operation

Each GP timer has four possible modes of operation:

- Stop/Hold mode
- Continuous Up-Counting mode
- Directional Up-/Down-Counting mode
- Continuous Up-/Down-Counting mode

The bit pattern in the corresponding timer control register TxCON determines the counting mode of a GP timer. The timer enabling bit, TxCON, enables or disables the counting operation of a timer. When the timer is disabled, the counting operation of the timer stops and the prescaler of the timer is reset to x/1. When the timer is enabled, the timer starts counting according to the counting mode specified by other bits of TxCON.

Stop/Hold Mode

In this mode the GP timer stops and holds at its current state. The timer counter, the compare output, and the prescale counter all remain unchanged in this mode.

Continuous Up-Counting Mode

The GP timer in this mode counts up according to the scaled input clock until the value of the timer counter matches that of the period register. On the next rising edge of the input clock after the match, the GP timer resets to zero and starts counting up again. The period interrupt flag of the timer is set one clock cycle after the match between the timer counter and period register. A peripheral interrupt request is generated if the flag is not masked.

An ADC start is sent to the ADC module at the same time the flag is set, if the period interrupt of this timer has been
selected by the appropriate bits in GPTCONA/B to start the ADC.
One clock cycle after the GP timer becomes 0, the underflow interrupt flag of the timer is set. A peripheral interrupt request is generated by the flag if it is unmasked. An ADC start is sent to the ADC module at the same time if the underflow interrupt flag of this timer has been selected by appropriate bits in GPTCONA/B to start ADC.
The overflow interrupt flag is set one clock cycle after the value in TxCNT matches FFFFh. A peripheral interrupt request is generated by the flag if it is unmasked. The duration of the timer period is (TxPR) + 1 cycles of the scaled clock input except for the first period. The duration of the first period is the same if the timer counter is zero when counting starts.
The initial value of the GP timer can be any value between 0h and FFFFh inclusive. When the initial value is greater than the value in the period register, the timer counts up to FFFFh, resets to zero, and continues the operation as if the initial value was zero. When the initial value in the timer counter is the same as that of the period register, the timer sets the period interrupt flag, resets to zero, sets the underflow interrupt flag, and then continues the operation again as if the initial value was zero. If the initial value of the timer is between zero and the contents of the period register, the timer counts up to the period value and continue to finish the period as if the initial counter value was the same as that of the period register.
The counting direction indication bit in GPTCONA/B is one for the timer in this mode. Either the external or internal device clock can be selected as the input clock to the timer. TDIRA/B input is ignored by the GP timer in this counting mode.
The continuous up-counting mode of the GP timer is particularly useful for the generation of edge-triggered or asynchronous PWM waveforms and sampling periods in many motor and motion control systems.

Directional Up-/Down-Counting Mode
The GP timer in directional up-/down-counting mode counts up or down according to the scaled clock and TDIRA/B inputs. The GP timer starts counting up until its value reaches that of the period register (or FFFFh if the initial count is greater than the period) when the TDIRA/B pin is held high. When the timer value equals that of its period register (or FFFFh) the timer resets to zero and continues counting up to the period again. When TDIRA/B is held low, the GP timer counts down until its value becomes zero. When the value of the timer has counted down to zero, the timer reloads its counter with the value in the period register and starts counting down again. The initial value of the timer can be any value between 0000h to FFFFh. When the initial value of the timer counter is greater than that of the period register, the timer counts up to FFFFh before resetting itself to zero and counting up to the period. If TDIRA/B is low when the timer starts with a value greater than the period register, it counts down to the value of the period register and continues counting down to zero, at which point the timer counter gets reloaded with the value from the period register as normal. The period, underflow, and overflow interrupt flags, interrupts, and associated actions are generated on respective events in the same manner as they are generated in the continuous up-counting mode.

The direction of counting is indicated for the timer in this mode by the corresponding direction indication bit in GPTCONA/B: 1 means counting up; 0 means counting down. Either the external clock from the TCLKINA/B pin or the internal device clock can be used as the input clock for the timer in this mode.
The directional up-/down-counting mode of GP timer 2/4 can be used with the quadrature encoder pulse (QEP) circuits in the EV module. The QEP circuits provide both the counting clock and direction for GP timer 2/4 in this case. This mode of operation can also be used to time the occurrence of external events in motion/motor control and power electronics applications.

Continuous Up-/Down-Counting Mode
This mode of operation is the same as the directional up-/down-counting mode, but the TDIRA/B pin has no effect on the counting direction. The counting direction only changes from up to down when the timer reaches the period value (or FFFFh if the initial timer value is greater than the period). The timer direction only changes from down to up when the timer reaches zero. The period of the timer in this mode is 2*(TxPR) cycles of the scaled clock input, except for the first period. The duration of the first counting period is the same if the timer counter is zero when counting starts. The initial value of the GP timer counter can be any value between 0h and FFFFh inclusive. When the initial value is greater than that of the period register, the timer counts up to FFFFh, resets to zero, and continues the operation as if the initial value was zero. When the initial value in the timer counter is the same as that of the period register, the timer counts down to zero and continues again as if the initial value was zero. If the initial value of the timer is between zero and the contents of the period register, the timer counts up to the period value and continues to finish the period as if the initial counter value was the same as that of the period register. The period, underflow, and overflow interrupt flags, interrupts, and associated actions are generated on respective events in the same manner as they are generated in continuous up-counting mode.
The counting direction indication bit for this timer in GPTCONA/B is one when the timer counts upward and zero when the timer counts downward. Either the external clock from the TCLKINA/B pin or the internal device clock can be selected as the input clock. TDIRA/B input is ignored by the timer in this mode.

1.5 GP Timer Compare Operation

Each GP timer has an associated compare register TxCMPR and a PWM output pin TxPWM. The value of a GP timer counter is constantly compared to that of its associated compare register. A compare match occurs when the value of the timer counter is the same as that of the compare register. Compare operation is enabled by setting TxCON to one. If it is enabled, the following happens on a compare match:
- The compare interrupt flag of the timer is set one clock cycle after the match
- A transition occurs on the associated PWM output according to the bit con-figuration in GPTCONA/B, one device clock cycle after the match
- If the compare interrupt flag has been selected by the appropriate GPTCONA/B bits to start ADC, an ADC start signal is generated at the same time the compare interrupt flag is

set. A peripheral interrupt request is generated by the compare interrupt flag if it is unmasked.

PWM Transition
The transition on the PWM output is controlled by an asymmetric and symmetric waveform generator and the associated output logic, and depends on the following:
- Bit definition in GPTCONA/B
- Counting mode the timer is in
- Counting direction when the counting mode is continuous-up/-down mode

1.6 Timer Control Registers (TxCON and GPTCONA/B)

The bit definition of the individual GP timer control registers, TxCON, is shown in the Figure below. The bit definition of the overall GP timer control registers, GPTCONA and GPTCONB, are shown in figures below.

Individual GP Timer Control Register (TxCON; x = 1, 2, 3, or 4)
Note:
Each Timer Control Register (TxCON) is independently configurable.

Timer x Control Register (TxCON; x = 1, 2, 3, or 4)

15	14	13	12	11	10	9	8
Free	Soft	Reserved	TMODE1	TMODE0	TPS2	TPS1	TPS0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
7	6	5	4	3	2	1	0
T2SWT1/ T4SWT3†	TENABLE	TCLKS1	TCLKS0	TCLD1	TCLD0	TECMPR	SELT1PR/ SELT3PR†
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

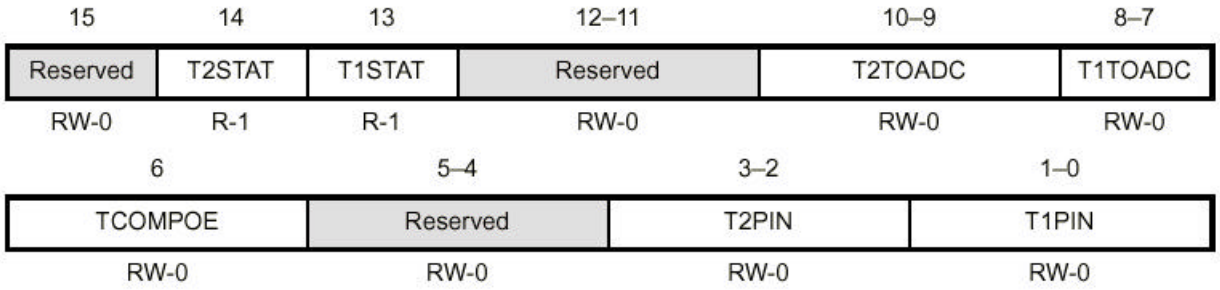
Note: R = Read access, W = Write access, -0 = value after reset
† Reserved in T1CON andT3CON

Bits 15–14 Free, Soft
Emulation control bits.
00 Stop immediately on emulation suspend
01 Stop after current timer period is complete on emulation suspend
10 Operation is not affected by emulation suspend
11 Operation is not affected by emulation suspend
Bit 13 Reserved
Reads return zero, writes have no effect.
Bits 12–11 TMODE1–TMODE0
Count Mode Selection.
00 Stop/Hold
01 Continuous-Up/-Down Count Mode
10 Continuous-Up Count Mode
11 Directional-Up/-Down Count Mode

Bits 10–8 TPS2–TPS0
Input Clock Prescaler.
000 x/1 100 x/16
001 x/2 101 x/32
010 x/4 110 x/64
011 x/8 111 x/128
x = device (CPU) clock frequency
Bit 7 T2SWT1
In the case of EVA, this bit is T2SWT1. (GP timer 2 start with GP timer 1.) Start GP timer 2 with GP timer 1's timer enable bit. This bit is reserved in T1CON.
T4SWT3
In the case of EVB, this bit is T4SWT3. (GP timer 4 start with GP timer 3.) Start GP timer 4 with GP timer 3's timer enable bit. This bit is reserved in T3CON.
0 Use own TENABLE bit
1 Use TENABLE bit of T1CON (in case of EVA) or T3CON (in case of EVB) to enable and disable operation ignoring own TENABLE bit
Bit 6 TENABLE
Timer enable.
0 Disable timer operation (the timer is put in hold and the prescaler counter is reset)
1 Enable timer operations
Bits 5–4 TCLKS1, TCLKS0
Clock Source Select.
0 0 Internal
0 1 External
1 0 Reserved
1 1 QEP Circuit † (in case of Timer 2/Timer 4)
Reserved (in case of Timer 1/Timer 3)
† This option is valid only if SELT1PR = 0
Bits 3–2 TCLD1, TCLD0
Timer Compare Register Reload Condition.
00 When counter is 0
01 When counter value is 0 or equals period register value
10 Immediately
11 Reserved
Bit 1 TECMPR
Timer compare enable.
0 Disable timer compare operation
1 Enable timer compare operation
Bit 0 SELT1PR
In the case of EVA, this bit is SELT1PR (Period register select).
When set to1 in T2CON, the period register of Timer 1 is chosen for Timer 2 also, ignoring the period register of Timer 2. This bit is a reserved bit in T1CON.
SELT3PR
In the case of EVB, this bit is SELT3PR (Period register select).
When set to1 in T4CON, the period register of Timer 3 is chosen for Timer 4 also, ignoring the period register of Timer 4. This bit is a reserved bit in T3CON.

0 Use own period register
1 Use T1PR (in case of EVA) or T3PR (in case of EVB) as period register ignoring own period register

GP Timer Control Register A (GPTCONA)

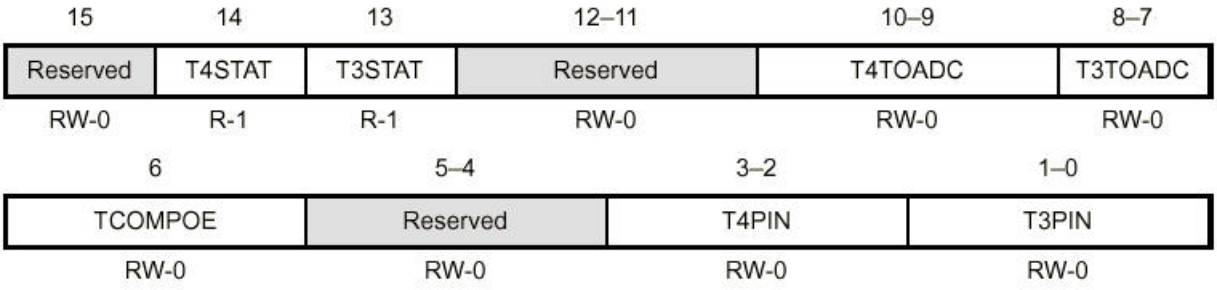


Note: R = Read access, W = Write access, -n = value after reset

Bit 15 Reserved
Reads return zero; writes have no effect.
Bit 14 T2STAT
GP timer 2 Status. Read only.
0 Counting downward
1 Counting upward
Bit 13 T1STAT
GP timer 1 Status. Read only.
0 Counting downward
1 Counting upward
Bits 12–11 Reserved
Reads return zero; writes have no effect.
Bits 10–9 T2TOADC
Start ADC with timer 2 event.
00 No event starts ADC
01 Setting of underflow interrupt flag starts ADC
10 Setting of period interrupt flag starts ADC
11 Setting of compare interrupt flag starts ADC
Bits 8–7 T1TOADC
Start ADC with timer 1 event.
00 No event starts ADC
01 Setting of underflow interrupt flag starts ADC
10 Setting of period interrupt flag starts ADC
11 Setting of compare interrupt flag starts ADC
Bit 6 TCOMPOE
Compare output enable. If PDPINTx is active this bit is set to zero.
0 Disable all GP timer compare outputs (all compare outputs are put in the high-impedance state)
1 Enable all GP timer compare outputs
Bits 5–4 Reserved
Reads return zero; writes have no effect.

Bits 3–2 T2PIN
Polarity of GP timer 2 compare output.
00 Forced low
01 Active low
10 Active high
11 Forced high
Bits 1–0 T1PIN
Polarity of GP timer 1 compare output.
00 Forced low
01 Active low
10 Active high
11 Forced high

GP Timer Control Register B (GPTCONB)



Note: R = Read access, W = Write access, -n = value after reset

Bit 15 Reserved
Reads return zero; writes have no effect.
Bit 14 T4STAT
GP timer 4 Status. Read only.
0 Counting downward
1 Counting upward
Bit 13 T3STAT
GP timer 3 Status. Read only.
0 Counting downward
1 Counting upward
Bits 12–11 Reserved
Reads return zero; writes have no effect.
Bits 10–9 T4TOADC
Start ADC with timer 4 event.
00 No event starts ADC
01 Setting of underflow interrupt flag starts ADC
10 Setting of period interrupt flag starts ADC
11 Setting of compare interrupt flag starts ADC
Bits 8–7 T3TOADC
Start ADC with timer 3 event.
00 No event starts ADC
01 Setting of underflow interrupt flag starts ADC

10 Setting of period interrupt flag starts ADC
11 Setting of compare interrupt flag starts ADC

Bit 6 TCOMPOE

Compare output enable. If PDPINTx is active this bit is set to zero.
0 Disable all GP timer compare outputs (all compare outputs are put in the high-impedance state)
1 Enable all GP timer compare outputs

Bits 5–4 Reserved

Reads return zero; writes have no effect.

Bits 3–2 T4PIN

Polarity of GP timer 4 compare output.
00 Forced low
01 Active low
10 Active high
11 Forced high

Bits 1–0 T3PIN

Polarity of GP timer 3 compare output.
00 Forced low
01 Active low
10 Active high
11 Forced high

1.7 Generation of PWM Outputs Using the GP Timers

Each GP timer can independently be used to provide a PWM output channel. Thus, up to two PWM outputs may be generated by the GP timers.

PWM Operation

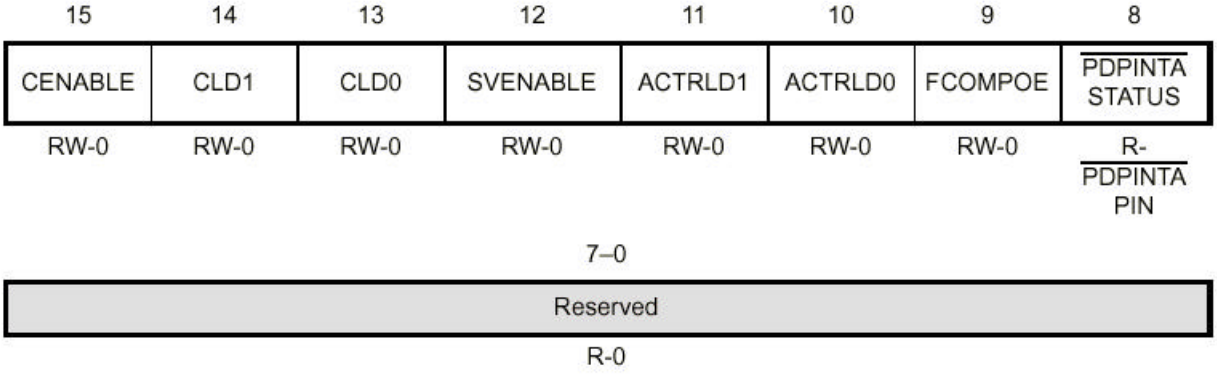
To generate a PWM output with a GP timer, a continuous up- or up-/down-counting mode can be selected. Edge-triggered or asymmetric PWM waveforms are generated when a continuous-up count mode is selected. Centered or symmetric PWM waveforms are generated when a continuous-up/-down mode is selected. To set up the GP timer for the PWM operation, do the following:
- Set up TxPR according to the desired PWM (carrier) period
- Set up TxCON to specify the counting mode and clock source, and start the operation
- Load TxCMPR with values corresponding to the on-line calculated widths (duty cycles) of PWM pulses

The period value is obtained by dividing the desired PWM period by the period of the GP timer input clock, and subtracting one from the resulting number when the continuous up-counting mode is selected to generate asymmetric PWM waveforms. When the continuous up-/down-counting mode is selected to generate symmetric PWM waveforms, this value is obtained by dividing the desired PWM period by two times the period of the GP timer input clock. The GP timer can be initialized the same way as in the previous example. During run time, the GP timer compare register is constantly updated with newly determined compare values corresponding to the newly determined duty cycles.

1.8 Compare Units Registers

Compare Control Registers (COMCONA and COMCONB)
The operation of the compare units is controlled by the compare control registers (COMCONA and COMCONB). The bit definition of COMCONA and COMCONB are summarized in the Figures below.
COMCONA and COMCONB are readable and writeable.

Compare Control Register A (COMCONA)

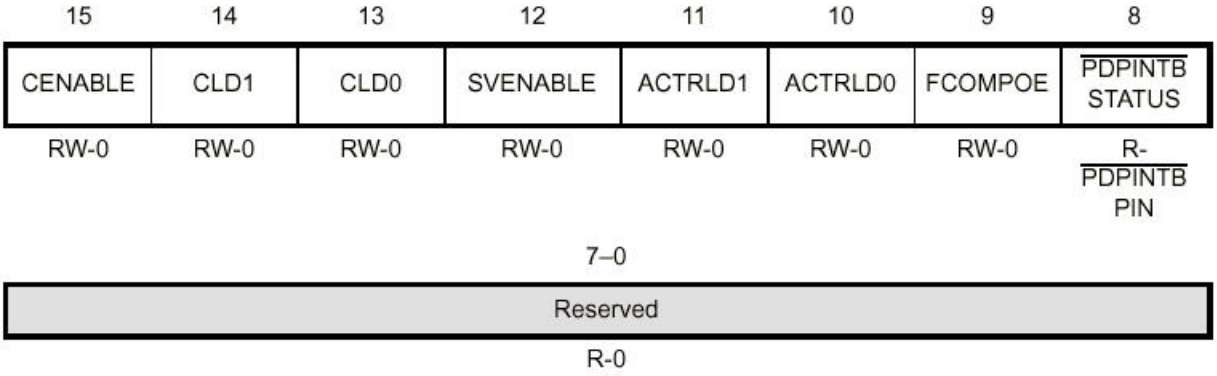


Note: R = Read access, W = Write access, -0 = value after reset

Bit 15 CENABLE
Compare enable.
0 Disables compare operation. All shadowed registers (CMPRx, ACTRA) become transparent
1 Enables compare operation
Bits14–13 CLD1, CLD0
Compare register CMPRx reload condition.
00 When T1CNT = 0 (that is, on underflow)
01 When T1CNT = 0 or T1CNT = T1PR (that is, on underflow or period match)
10 Immediately
11 Reserved; result is unpredictable
Bit 12 SVENABLE
Space vector PWM mode enable.
0 Disables space vector PWM mode
1 Enables space vector PWM mode
Bits 11–10 ACTRLD1, ACTRLD0
Action control register reload condition.
00 When T1CNT = 0 (on underflow)
01 When T1CNT = 0 or T1CNT = T1PR (on underflow or period match)
10 Immediately
11 Reserved
Bit 9 FCOMPOE
Compare output enable. Active PDPINTA clears this bit to zero.
0 PWM output pins are in high-impedance state; that is, they are disabled
1 PWM output pins are not in high-impedance state; that is, they are enabled

Bit 8 PDPINTA STATUS
This bit is reserved on 2407 (DSP we will be using in EE757) devices.
Bits 7–0 Reserved
Read returns zero; writes have no effect.

Compare Control Register B (COMCONB)



Note: R = Read access, W = Write access, -0 = value after reset

Bit 15 CENABLE
Compare enable.
0 Disable compare operation. All shadowed registers (CMPRx, ACTRB) become transparent
1 Enable compare operation
Bits14–13 CLD1, CLD0
Compare register CMPRx reload condition.
00 When T3CNT = 0 (that is, on underflow)
01 When T3CNT = 0 or T3CNT = T3PR (that is, on underflow or period match)
10 Immediately
11 Reserved; result is unpredictable
Bit 12 SVENABLE
Space vector PWM mode enable.
0 Disables space vector PWM mode
1 Enables space vector PWM mode
Bits 11–10 ACTRLD1, ACTRLD0
Action control register reload condition.
00 When T3CNT = 0 (on underflow)
01 When T3CNT = 0 or T3CNT = T3PR (on underflow or period match)
10 Immediately
11 Reserved
Bit 9 FCOMPOE
Compare output enable. Active PDPINTB clears this bit to zero.
0 PWM output pins are in high-impedance state; that is, they are disabled
1 PWM output pins are not in high-impedance state; that is, they are enabled
Bit 8 PDPINTB STATUS
This bit is reserved on 2407 (DSP we will be using in EE757) devices.

Bits 7–0 Reserved
Read returns zero; writes have no effect.

Compare Action Control Registers (ACTRA and ACTRB)
The compare action control registers (ACTRA and ACTRB) control the action that takes place on each of the six compare output pins (PWMx, where x = 1–6 for ACTRA, and x = 7–12 for ACTRB) on a compare event, if the compare operation is enabled by COMCONx. ACTRA and ACTRB are double-buffered. The condition on which ACTRA and ACTRB is reloaded is defined by bits in COMCONx. ACTRA and ACTRB also contain the SVRDIR, D2, D1, and D0 bits needed for space vector PWM operation. The bit configuration of ACTRA and ACTRB are described in the Figures below.

Compare Action Control Register A (ACTRA)

15	14	13	12	11	10	9	8
SVRDIR	D2	D1	D0	CMP6ACT1	CMP6ACT0	CMP5ACT1	CMP5ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
7	6	5	4	3	2	1	0
CMP4ACT1	CMP4ACT0	CMP3ACT1	CMP3ACT0	CMP2ACT1	CMP2ACT0	CMP1ACT1	CMP1ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

Note: R = Read access, W = Write access, -0 = value after reset

Bit 15 SVRDIR
Space vector PWM rotation direction. Used only in space vector PWM output generation.
0 Positive (CCW)
1 Negative (CW)
Bits 14–12 D2–D0
Basic space vector bits. Used only in space vector PWM output generation.
Bits 11–10 CMP6ACT1–0
Action on compare output pin 6, CMP6.
00 Forced low
01 Active low
10 Active high
11 Forced high
Bits 9–8 CMP5ACT1–0
Action on compare output pin 5, CMP5.
00 Forced low
01 Active low
10 Active high
11 Forced high
Bits 7–6 CMP4ACT1–0
Action on compare output pin 4, CMP4.
00 Forced low
01 Active low
10 Active high
11 Forced high

Bits 5–4 CMP3ACT1–0
Action on compare output pin 3, CMP3.
00 Forced low
01 Active low
10 Active high
11 Forced high
Bits 3–2 CMP2ACT1–0
Action on compare output pin 2, CMP2.
00 Forced low
01 Active low
10 Active high
11 Forced high
Bits 1–0 CMP1ACT1–0
Action on compare output pin 1, CMP1.
00 Forced low
01 Active low
10 Active high
11 Forced high

Compare Action Control Register B (ACTRB)

15	14	13	12	11	10	9	8
SVRDIR	D2	D1	D0	CMP12ACT1	CMP12ACT0	CMP11ACT1	CMP11ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
7	6	5	4	3	2	1	0
CMP10ACT1	CMP10ACT0	CMP9ACT1	CMP9ACT0	CMP8ACT1	CMP8ACT0	CMP7ACT1	CMP7ACT0
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

Note: R = Read access, W = Write access, -0 = value after reset

Bit 15 SVRDIR
Space vector PWM rotation direction. Used only in space vector PWM output generation.
0 Positive (CCW)
1 Negative (CW)
Bits 14–12 D2–D0
Basic space vector bits. Used only in space vector PWM output generation.
Bits 11–10 CMP12ACT1–0
Action on compare output pin 12, CMP12.
00 Forced low
01 Active low
10 Active high
11 Forced high
Bits 9–8 CMP11ACT1–0
Action on compare output pin 11, CMP11.
00 Forced low
01 Active low
10 Active high

11 Forced high
Bits 7–6 CMP10ACT1–0
Action on compare output pin 10, CMP10.
00 Forced low
01 Active low
10 Active high
11 Forced high
Bits 5–4 CMP9ACT1–0
Action on compare output pin 9, CMP9.
00 Forced low
01 Active low
10 Active high
11 Forced high
Bits 3–2 CMP8ACT1–0
Action on compare output pin 8, CMP8.
00 Forced low
01 Active low
10 Active high
11 Forced high
Bits 1–0 CMP7ACT1–0
Action on compare output pin 7, CMP7.
00 Forced low
01 Active low
10 Active high
11 Forced high

1.9 Compare Unit Interrupts

There is a maskable interrupt flag in EVIFRA and EVIFRC for each compare unit. The interrupt flag of a compare unit is set one clock cycle after a compare match, if a compare operation is enabled. A peripheral interrupt request is generated by the flag if it is unmasked.

2. PWM Waveform Generation With Compare Units and PWM Circuits

A pulse width modulated (PWM) signal is a sequence of pulses with changing pulse widths. The pulses are spread over a number of fixed-length periods so that there is one pulse in each period. The fixed period is called the PWM (carrier) period and its inverse is called the PWM (carrier) frequency. The widths of the PWM pulses are determined, or modulated, from pulse to pulse according to another sequence of desired values, the modulating signal. In a motor control system, PWM signals are used to control the on and off time of switching power devices that deliver the desired current and energy to the motor windings. The shape and frequency of the phase currents and the amount of energy delivered to the motor windings control the required speed and torque of the motor. In this case, the command voltage or current to be applied to the motor is the modulating

signal. The frequency of the modulating signal is typically much lower than the PWM carrier frequency.

PWM Signal Generation
To generate a PWM signal, an appropriate timer is needed to repeat a counting period that is the same as the PWM period. A compare register is used to hold the modulating values. The value of the compare register is constantly compared with the value of the timer counter. When the values match, a transition (from low to high, or high to low) happens on the associated output. When a second match is made between the values, or when the end of a timer period is reached, another transition (from high to low, or low to high) happens on the associated output. In this way, an output pulse is generated whose on (or off) duration is proportional to the value in the compare register. This process is repeated for each timer period with different (modulating) values in the compare register. As a result, a PWM signal is generated at the associated output.

2.1 Generation of PWM Outputs With Event Manager

Each of the three compare units, together with GP timer 1 (in the case of EVA) or GP timer 3 (in the case of EVB), the dead-band unit, and the output logic in the event manager module, can be used to generate a pair of PWM outputs. There are six such dedicated PWM output pins associated with the three compare units in each EV module. Each GP timer compare unit, if desired, can also generate a PWM output based on its own timer.

Asymmetric and Symmetric PWM Generation
Both asymmetric and symmetric PWM waveforms can be generated by every compare unit on the EV module. PWM generation with GP timer compare units has been described in the GP timer sections. Generation of PWM outputs with the compare units is discussed in this section.

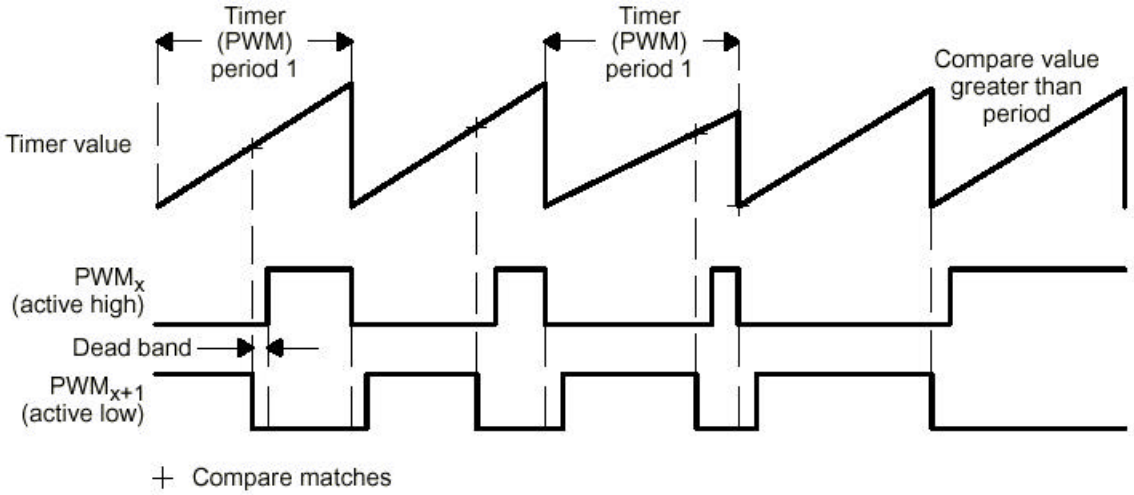
2.2 Register Setup for PWM Generation

All three kinds of PWM waveform generations with compare units and associated circuits require configuration of the same Event Manager registers. The setup process for PWM generation includes the following steps:
- Setup and load ACTRx
- Setup and load DBTCONx, if dead-band is to be used (in EE757 experiments, dead-band won't be used.)
- Initialize CMPRx
- Setup and load COMCONx
- Setup and load T1CON (for EVA) or T3CON (for EVB) to start the operation
- Rewrite CMPRx with newly determined values

2.3 Asymmetric PWM Waveform Generation

The edge-triggered or asymmetric PWM signal is characterized by modulated pulses which are not centered with respect to the PWM period, as shown in the figure below. The width of each pulse can only be changed from one side of the pulse.

Asymmetric PWM Waveform Generation With Compare Unit and PWM Circuits (x = 1, 3, or 5)



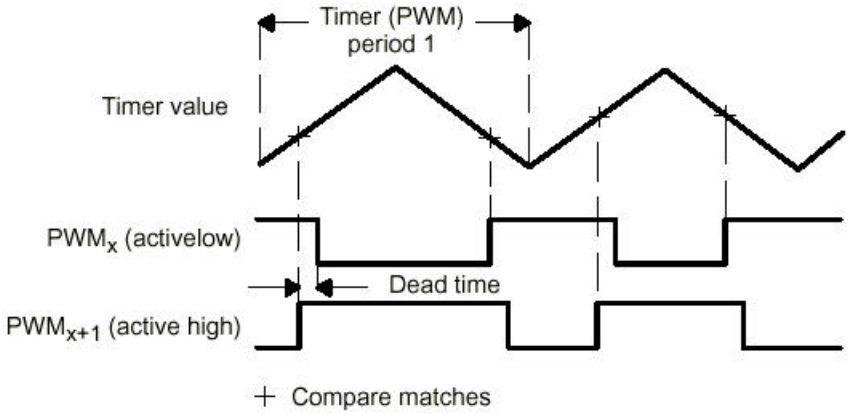
To generate an Asymmetric PWM signal, GP timer 1 is put in the continuous up-counting mode and its period register is loaded with a value corresponding to the desired PWM carrier period. The COMCONx is configured to enable the compare operation, set the selected output pins to be PWM outputs, and enable the outputs. By proper configuration of ACTRx with software, a normal PWM signal can be generated on one output associated with a compare unit while the other is held low (or off) or high (or on), at the beginning, middle, or end of a PWM period.

After GP timer 1 (or GP timer 3) is started, the compare registers are rewritten every PWM period with newly determined compare values to adjust the width (the duty cycle) of PWM outputs that control the switch-on and -off duration of the power devices. Since the compare registers are shadowed, a new value can be written to them at any time during a period. For the same reason, new values can be written to the action and period registers at any time during a period to change the PWM period or to force changes in the PWM output definition.

2.4 Symmetric PWM Waveform Generation

A centered or symmetric PWM signal is characterized by modulated pulses which are centered with respect to each PWM period. The advantage of a symmetric PWM signal over an asymmetric PWM signal is that it has two inactive zones of the same duration: at the beginning and at the end of each PWM period. The figure below shows two examples of symmetric PWM waveforms.

Symmetric PWM Waveform Generation With Compare Units and PWM Circuits (x = 1, 3, or 5)



The generation of a symmetric PWM waveform with a compare unit is similar to the generation of an asymmetric PWM waveform. The only exception is that GP timer 1 (or GP timer 3) now needs to be put in continuous up-/down-counting mode.
There are usually two compare matches in a PWM period in symmetric PWM waveform generation, one during the upward counting before period match, and another during downward counting after period match. A new compare value becomes effective after the period match (reload on period) because it makes it possible to advance or delay the second edge of a PWM pulse. Because the compare registers are shadowed, a new value can be written to them at any time during a period. For the same reason, new values can be written to the action and period registers at any time during a period to change the PWM period or to force changes in the PWM output definition.

3. Capture Units

Capture units enable logging of transitions on capture input pins. There are six capture units, three is each EV module. Capture Units 1, 2, and 3 are associated with EVA and Capture Units 4, 5, and 6 are associated with EVB. Each capture unit is associated with a capture input pin. Each EVA capture unit can choose GP timer 2 or 1 as its time base; however, CAP1 and CAP2 cannot choose a different timer between themselves as their timebase. Each EVB capture unit can choose GP timer 4 or 3 as its time base; however, CAP4 and CAP5 cannot choose a different timer between themselves as their timebase. The value of the GP timer is captured and stored in the corresponding 2-leveldeep FIFO stack when a specified transition is detected on a capture input pin (CAPx).

Capture units have the following features:
- One 16-bit capture control register (CAPCONA for EVA, CAPCONB for EVB), (RW)
- One 16-bit capture FIFO status register (CAPFIFOA for EVA, CAPFIFOB for EVB)
- Selection of GP timer 1 or 2 (for EVA) and GP timer 3 or 4 (for EVB) as the time base
- Three 16-bit 2-level-deep FIFO stacks, one for each capture unit
- Six Schmitt-triggered capture input pins, CAP1 through CAP6, one input pin for each capture unit. (All inputs are synchronized with the device/CPU clock: in order for a transition to be captured, the input must hold at its current level to meet the two rising edges of the device clock. Input pins CAP1 and CAP2 (CAP4 and CAP5 in case of EVB) can also be used as QEP inputs to QEP circuit)
- User-specified transition detection (rising edge, falling edge, or both edges)
- Six maskable interrupt flags, one for each capture unit

3.1 Operation of Capture Units

After a capture unit is enabled, a specified transition on the associated input pin causes the counter value of the selected GP timer to be loaded into the corresponding FIFO stack. At the same time, if there are already one or more valid capture values stored in the FIFO stack (CAPxFIFO bits not equal to zero), the corresponding interrupt flag is set. If the flag is unmasked, a peripheral interrupt request is generated. The corresponding status bits in CAPFIFOx are adjusted to reflect the new status of the FIFO stack each time a new counter value is captured in a FIFO stack. The latency from the time a transition happens in a capture input to the time the counter value of the selected GP timer is locked is two clock cycles. All capture unit registers are cleared to zero by a RESET condition.

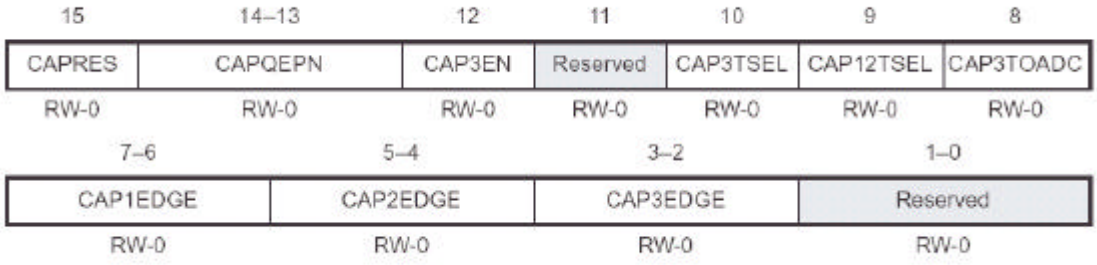
Capture Unit Time Base Selection
For EVA, Capture Unit 3 has a separate time base selection bit from Capture Units 1 and 2. This allows the two GP timers to be used at the same time, one for Capture Units 1 and 2, and the other for Capture Unit 3. For EVB, Capture Unit 6 has a separate time base selection bit. Capture operation does not affect the operation of any GP timer or the compare/PWM operations associated with any GP timer.

Capture Unit Setup
For a capture unit to function properly, the following register setup must be performed:
1) Initialize the CAPFIFOx and clear the appropriate status bits.
2) Set the selected GP timer in one of its operating modes.
3) Set the associated GP timer compare register or GP timer period register, if necessary.
4) Set up CAPCONA or CAPCONB as appropriate.

3.2 Capture Unit Registers

The operation of the capture units is controlled by four 16-bit control registers, CAPCONA/B and CAPFIFOA/B. TxCON (x = 1, 2, 3, or 4) registers are also used to control the operation of the capture units since the time base for capture circuits can be provided by any of these timers. Additionally, CAPCONA/B is also used to control the operation of the QEP circuit.

Capture Control Register A (CAPCONA)



Note: R = Read access, W = Write access, -0 = value after reset

Bit 15 CAPRES
Capture reset. Always reads zero.
Note: This bit is not implemented as a register bit. Writing a 0 simply clears the capture registers.
0 Clear all registers of capture units and QEP circuit to 0
1 No action

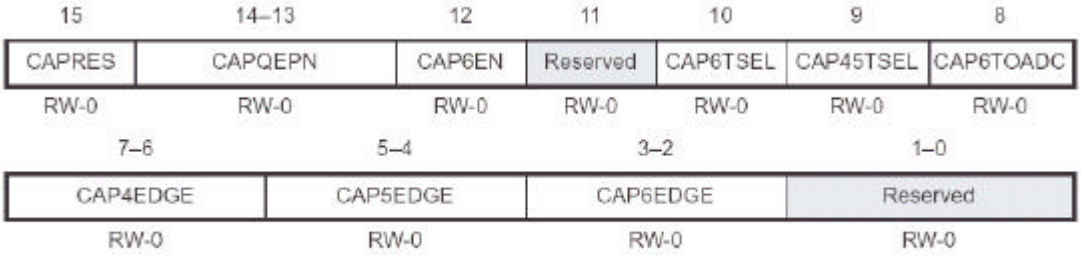
Bits 14–13 CAPQEPN
Capture Units 1 and 2 control.
00 Disables Capture Units 1 and 2; FIFO stacks retain their contents
01 Enables Capture Units 1 and 2
10 Reserved
11 Reserved

Bit 12 CAP3EN
Capture Unit 3 control.
0 Disables Capture Unit 3; FIFO stack of Capture Unit 3 retains its contents
1 Enable Capture Unit 3

Bit 11 Reserved
Reads return zero; writes have no effect.

Bit 10 CAP3TSEL
GP timer selection for Capture Unit 3.
0 Selects GP timer 2
1 Selects GP timer 1
Bit 9 CAP12TSEL
GP timer selection for Capture Units 1 and 2.
0 Selects GP timer 2
1 Selects GP timer 1
Bit 8 CAP3TOADC
Capture Unit 3 event starts ADC.
0 No action
1 Starts ADC when the CAP3INT flag is set
Bits 7–6 CAP1EDGE
Edge detection control for Capture Unit 1.
00 No detection
01 Detects rising edge
10 Detects falling edge
11 Detects both edges
Bits 5–4 CAP2EDGE
Edge detection control for Capture Unit 2.
00 No detection
01 Detects rising edge
10 Detects falling edge
11 Detects both edges
Bits 3–2 CAP3EDGE
Edge detection control for Capture Unit 3.
00 No detection
01 Detects rising edge
10 Detects falling edge
11 Detects both edges
Bits 1–0 Reserved
Reads return zero; writes have no effect.

Capture Control Register B (CAPCONB)



Note: R = Read access, W = Write access, -0 = value after reset

Bit 15 CAPRES
Capture reset. Always reads zero.
Note: This bit is not implemented as a register bit. Writing a 0 simply clears the capture registers.
0 Clears all registers of capture units and QEP circuit to 0
1 No action
Bits 14–13 CAPQEPN
Capture Units 4 and 5 and QEP circuit control.
00 Disables Capture Units 4 and 5 and QEP circuit. FIFO stacks retain their contents
01 Enables Capture Units 4 and 5, disable QEP circuit
10 Reserved
11 Enables QEP circuit. Disable Capture Units 4 and 5; bits 4–7 and 9 are ignored
Bit 12 CAP6EN
Capture Unit 6 control.
0 Disables Capture Unit 6; FIFO stack of Capture Unit 6 retains its contents
1 Enables Capture Unit 6
Bit 11 Reserved
Reads return zero; writes have no effect.
Bit 10 CAP6TSEL
GP timer selection for Capture Unit 6.
0 Selects GP timer 4
1 Selects GP timer 3
Bit 9 CAP45TSEL
GP timer selection for Capture Units 4 and 5.
0 Selects GP timer 4
1 Selects GP timer 3
Bit 8 CAP6TOADC
Capture Unit 6 event starts ADC.
0 No action
1 Starts ADC when the CAP6INT flag is set
Bits 7–6 CAP4EDGE
Edge detection control for Capture Unit 4.
00 No detection
01 Detects rising edge
10 Detects falling edge

Reads return zero; writes have no effect.

Bits 13–12 CAP3FIFO

CAP3FIFO Status.

00 Empty

01 Has one entry

10 Has two entries

11 Had two entries and captured another one; first entry has been lost

Bits 11–10 CAP2FIFO

CAP2FIFO Status

00 Empty

. Reads return zero; writes have no effect.

Bits 13–12 CAP6FIFO. CAP6FIFO Status.

00 Empty

01 Has one entry

10 Has two entries

11 Had two entries and captured another one; first entry has been lost

Bits 11–10 CAP5FIFO. CAP5FIFO Status

00 Empty

01 Has one entry

10 Has two entries

11 Had two entries and captured another one; first entry has been lost

Bits 9–8 CAP4FIFO. CAP4FIFO Status.

00 Empty

01 Has one entry

10 Has two entries

11 Had two entries and captured another one; first entry has been lost

Bits 7–0 Reserved. Reads return zero; writes have no effect.

3.3 Capture Unit FIFO Stacks

Each capture unit has a dedicated 2-level-deep FIFO stack. The top stack consists of CAP1FIFO, CAP2FIFO, and CAP3FIFO (in the case of EVA) or CAP4FIFO, CAP5FIFO, and CAP6FIFO (in the case of EVB). The bottom stack consists of CAP1FBOT, CAP2FBOT, and CAP3FBOT (in the case of EVA) or CAP4FBOT, CAP5FBOT, and CAP6FBOT (in the case of EVB). The top-level register of any of the FIFO stacks is a read-only register that always contains the oldest counter value captured by the corresponding capture unit. Therefore, a read access to the FIFO stack of a capture unit always returns the oldest counter value stored in the stack. When the oldest counter value in the top register of the FIFO stack is read, the newer counter value in the bottom register of the stack, if any, is pushed into the top register. If desired, the bottom register of the FIFO stack can be read. Reading the bottom register of the FIFO stack causes the FIFO status bits to change to 01 (has one entry) if they were previously 10 or 11. If the FIFO status bits were previously 01 when the bottom FIFO register is read, they will change to 00 (empty).

First Capture
The counter value of the selected GP timer (captured by a capture unit when a specified transition happens on its input pin) is written into the top register of the FIFO stack, if the stack is empty. At the same time, the corresponding status bits are set to 01. The status bits are reset to 00 if a read access is made to the FIFO stack before another capture is made.

Second Capture
If another capture occurs before the previously captured counter value is read, the newly captured counter value goes to the bottom register. In the meantime, the corresponding status bits are set to 10. When the FIFO stack is read before another capture happens, the older counter value in the top register is read out, the newer counter value in the bottom register is pushed up into the top register, and the corresponding status bits are set to 01. The appropriate capture interrupt flag is set by the second capture. A peripheral interrupt request is generated if the interrupt is not masked.

Third Capture
If a capture happens when there are already two counter values captured in the FIFO stack, the oldest counter value in the top register of the stack is pushed out and lost, the counter value in the bottom register of the stack is pushed up into the top register, the newly captured counter value is written into the bottom register, and the status bits are set to 11 to indicate that one or more older captured counter values have been lost. The appropriate capture interrupt flag is also set by the third capture. A peripheral interrupt request is generated if the interrupt is not masked.

3.4 Capture Interrupt

When a capture is made by a capture unit and there is already at least one valid value in the FIFO (indicated by CAPxFIFO bits not equal to zero), the corresponding interrupt flag is set, and if unmasked, a peripheral interrupt request is generated. Thus, a pair of captured counter values can be read by an interrupt service routine if the interrupt is used. If an interrupt is not desired, either the interrupt flag or the status bits can be polled to determine if two captures have occurred allowing the captured counter values to be read.

4. Quadrature Encoder Pulse (QEP) Circuit

Each Event Manager module has a quadrature encoder pulse (QEP) circuit. The QEP circuit, when enabled, decodes and counts the quadrature encoded input pulses on pins CAP1/QEP1 and CAP2/QEP2 (in case of EVA) or CAP4/QEP3 and CAP5/QEP4 (in case of EVB). The QEP circuit can be used to interface with an optical encoder to get position and speed information from a rotating machine. When the QEP circuit is enabled, the capture function on CAP1/CAP2 and CAP4/CAP5 pins is disabled.

4.1 QEP Pins

The two QEP input pins are shared between capture units 1 and 2 (or 3 and 4, for EVB), and the QEP circuit. Proper configuration of CAPCONx bits is required to enable the QEP circuit and disable capture units, thus assigning the associated input pins for use by the QEP circuit.

4.2 QEP Circuit Time Base

The time base for the QEP circuit is provided by GP timer 2 (GP timer 4, in case of EVB). The GP timer must be put in directional-up/down count mode with the QEP circuit as the clock source.

4.3 Decoding

Quadrature encoded pulses are two sequences of pulses with a variable frequency and a fixed phase shift of a quarter of a period (90 degrees). When generated by an optical encoder on a motor shaft, the direction of rotation of the motor can be determined by detecting which of the two sequences is the leading sequence. The angular position and speed can be determined by the pulse count and pulse frequency.

QEP Circuit
The direction detection logic of the QEP circuit in the EV module determines which one of the sequences is the leading sequence. It then generates a direction signal as the direction input to GP timer 2 (or 4). The timer counts up if CAP1/QEP1 (CAP4/QEP3 for EVB) input is the leading sequence, and counts down if CAP2/QEP2 (CAP5/QEP4 for EVB) is the leading sequence. Both edges of the pulses of the two quadrature encoded inputs are counted by the QEP circuit. Therefore, the frequency of the clock generated by the QEP logic to GP timer 2 (or 4) is four times that of each input sequence. This quadrature clock is connected to the clock input of GP timer 2 (or 4).

4.4 QEP Counting

GP timer 2 (or 4) always starts counting from its current value. A desired value can be loaded to the GP timer's counter prior to enabling the QEP mode. When the QEP circuit is selected as the clock source, the timer ignores the TDIRA/B and TCLKINA/B input pins.

GP Timer Interrupt and Associated Compare Outputs in QEP Operation
Period, underflow, overflow, and compare interrupt flags for a GP timer with a QEP circuit clock, are generated on respective matches. A peripheral interrupt request can be generated by an interrupt flag, if the interrupt is unmasked.

4.5 Register Setup for the QEP Circuit

To start the operation of the QEP circuit in EVA:
1) Load GP timer 2's counter, period, and compare registers with desired values, if necessary.
2) Configure T2CON to set GP timer 2 in directional-up/down mode with the QEP circuits as clock source, and enable the selected timer.
3) Configure CAPCONA to enable the QEP circuit.
To start the operation of the QEP circuit in EVB:
1) Load GP timer 4's counter, period, and compare registers with desired values, if necessary.
2) Configure T4CON to set GP timer 4 in directional-up/down mode with the QEP circuits as clock source, and enable the selected timer.
3) Configure CAPCONB to enable the QEP circuit.

5. Event Manager (EV) Interrupts

EV interrupt events are organized into three groups: A, B, and C. Each group is associated with a different interrupt flag and interrupt enable register. There are several event manager peripheral interrupt requests in each EV interrupt group. There is an interrupt flag register and a corresponding interrupt mask register for each EV interrupt group, as shown below. A flag in EVAIFRx (x = A, B, or C) is masked (will not generate a peripheral interrupt request) if the corresponding bit in EVAIMRx is zero.

Flag Register	**Mask Register**	**EV Module**
EVAIFRA	EVAIMRA	
EVAIFRB	EVAIMRB	EVA
EVAIFRC	EVAIMRC	
EVBIFRA	EVBIMRA	
EVBIFRB	EVBIMRB	EVB
EVBIFRC	EVBIMRC	

5.1 EV Interrupt Request and Service

When a peripheral interrupt request is acknowledged, the appropriate peripheral interrupt vector is loaded into the peripheral interrupt vector register (PIVR) by the PIE controller. The vector loaded into the PIVR is the vector for the highest priority pending enabled event. The vector register can be read by the interrupt service routine (ISR).

Event Manager A (EVA) Interrupts

Group	Interrupt	Priority within group	Vector(ID)	Description/Source	INT
	PDPINTA	1 (highest)	0020h	Power Drive Protection Interrupt A	1
A	CMP1INT	2	0021h	Compare Unit 1 compare interrupt	2
A	CMP2 INT	3	0022h	Compare Unit 2 compare interrupt	2
A	CMP3INT	4	0023h	Compare Unit 3 compare interrupt	2
A	T1PINT	5	0027h	GP timer 1 period interrupt 2	2
A	T1CINT	6	0028h	GP timer 1 compare interrupt	2
A	T1UFINT	7	0029h	GP timer 1 underflow interrupt	2
A	T1OFINT	8(lowest)	002Ah	GP timer 1 overflow interrupt	2
B	T2PINT	1 (highest)	002Bh	GP timer 2 period interrupt	3
B	T2CINT	2	002Ch	GP timer 2 compare interrupt	3
B	T2UFINT	3	002Dh	GP timer 2 underflow interrupt	3
B	T2OFINT	4	002Eh	GP timer 2 overflow interrupt	3
C	CAP1INT	1 (highest)	0033h	Capture Unit 1 interrupt	4
C	CAP2INT	2	0034h	Capture Unit 2 interrupt	4
C	CAP3INT	3	0035h	Capture Unit 3 interrupt	4