

**+ Project Assignment #1****DUE: Fri, Apr 4<sup>th</sup>**

Write a VHDL dataflow description for the 4 to 1 multiplexer where the G's are connected to the data inputs of the mux, and A and B are connected to the "select" or control inputs. In writing the logic equations for this unit think in terms of a 4-to-1 multiplexer. Then realize that A and B are the select inputs of the multiplexer and the truth table is connected to the G (or data) inputs. This is a 4 to 1 multiplexer or what we will call a "generic\_function unit".

The entity interface for it is:

```
ENTITY generic_function IS
  PORT( A, B, G3, G2, G1, G0 : IN BIT;
        R : OUT BIT);
END generic_function;
```

The 16 functions are:

(note that the G values are Hex)

<u>G3 G2 G1 G0</u>	<u>Function</u>
0	zero
1	NOR
2	A'B
3	A'
4	AB'
5	B'
6	XOR
7	NAND
8	AND
9	XNOR
A	B
B	A' + B
C	A
D	A + B'
E	OR
F	one

You can use concurrent signal assignment statement(s), a selected signal assignment statement, or a conditional signal assignment statement to write the model:

Concurrent signal assignment statement example:

```
Y <= (A AND B OR C) NOR D;
```

Conditional Signal Assignment Statement example (Navabi pages 207-209):

```
Y <= '1'      WHEN Q = "000" ELSE
  A AND C    WHEN Q = "001" ELSE
  A OR C     WHEN Q = "001" ELSE
  NOT C;
```

Selected Signal Assignment Statement example (Navabi page 272-275):

```
WITH bit_vector_signal SELECT
  Y <= '0' WHEN "0000",
      '1' WHEN "0010" | "0011",
      A  WHEN OTHERS;
```

To complete this class assignment:

- 1) Copy the file **pr\_step1.vhdl** from directory **~degroat/ee762\_assign** or download from the course website to your local directory.
- 2) Edit this file and enter your **architecture** for the generic function block. Note that an ENTITY declaration is already declared and completed. You will need to use the signal names declared in the ENTITY.
- 3) Compile the file.
- 4) Simulate the description using vsim. Note that you will select the testbench, **p1tb**, as the entity that you want to simulate. You do not select the architecture. Make sure you simulate it for all the test cases.
- 5) Turn in
  - a) copy of the code.
  - b) copy of a file listing the results of the simulation in tabular form.
  - c) copy of the waveform trace for the simulation. Be sure to print the entire simulation. You will need to simulate for 5200 ns so that all the test cases run.

NOTES:

No delay values are required for this simulation. You can try different values for delay if you like. If you use delays of more than 25ns from inputs to outputs you will get erroneous results as new test values are applied every 25 ns.

The order of analysis is important. You must compile the generic functional unit entity design unit, then its architecture, then the testbench entity and then the testbench architecture. By entering the architecture where indicated and analyzing this single file, the order of analysis will be correct.

In a previous version of the simulator, the testbench for this architecture stopped simulating when all vector were run. There is no longer a choice "Time'High" from the Run pulldown any more. So either select Run button until all vectors are run or run the simulation for 5200 ns.