PIPELINED FLOATING POINT

ADDER/MULTIPLIER

HDL Design and Verification Project

 This project is the culminating project for ECE 5462 this semester. I consists of several items that will be turned in.

 The Design Specification Document Due Friday November 13th

 The Verification Plan Due Friday November 17th

 The Design Report Due December 1st

 The Verification Report Due Wednesday December 6th

 The Project Oral Presentation Friday December 8 6-7:45pm

What are the documents?

 The Design Specification Document: This document specified what is being designed. In this case it is a pipelined floating point unit that has several internal stages. The logical points to put in the pipelined registers to create the pipeline stages are after the input manipulation and preparation for the operation. This involves taking the 32 bit input and separating out the exponent, sign, and mantissa along with generation of signals indicating aspects of the input.

 The next step is adding or multiplying the mantissas. This document will address how you intend to handle addition/multiplication to/by infinity and similar operations. The next pipeline stage is to do the renormalization. If you have time I will accept adding another pipeline stage to do rounding.

 The Verification Plan: This document is written early as you are doing the design and specifies how you are going to verify the design as it is being developed and when it is completed. Important parts are details on the testbench(s) to be built and what the condition is for moving on to the next step as the verification is consider successful.

 The Design Report: This document provides details of your specific design. It has all the HDL code of the design in the appendix. Note that you may want to create two HDL models. One is a high level reference model that is done algorithmically. It is used to create test vectors. The other is the synthesizable dataflow version.

 The Verification Report: This report details the verification plan execution. It details the results for all the subunit verification and the verification of the final design.

 The Project Oral Presentation: This is a presentation as you would have in your company so it needs to be effective. In a company not all members of the team necessarily speak. Those best at presenting do.

A block diagram of the floating point adder is given below.



For the multiplier you need to add the exponent sum to the input conditioning and pipeline it so it is available for the renormalization stage. For multiplication you also need to know things like an input is 0, infinity, or a NaN, just like in addition.

For the multiplier I suggest using a Booth multiplier. A regular Booth multiplier would have 24 stages and uses the multiplicand to determine if you add +m, do nothing, or add -m.

In a 2nd order Booth multiplier you would only have 12 stages and would be

Adding 2\*m, adding m, do nothing, adding –m, or adding –2\*m.

Wikipedia has a very good explanation of a Booth multiplier.

The normalization if the same for both addition and multiplication. In both cases, the inputs are in the range [0..2) and the output is in the range [0..4).