Autumn 2014 Material Covered ECE 5462

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|  | Cl | Covered | Assgn | Due |  |  |
| W | 1 | L1 – Course Intro | None |  |  |  |
|  | 2 | L2 – VHDL Intro and Homework 1 | HW1 | F 9/5 |  |  |
| W | 3 | L3 – Data Paths 1 |  |  |  |  |
|  | 4 | L4 – Data Paths 2 Project Step 1 | PS1 | W 9/10 |  |  |
| M | 5 | L5 – Lang OV I thru slide 15 |  |  |  |  |
|  | 6 | Lang OV I Thru slide 30 PS2 | PS2 | M 9/15 |  |  |
|  | 7 | Finish Lang OV I |  |  |  |  |
| M | 8 | Lang OV II thru to Seq - Slide 20 PS3 | PS3 | F 9/19 |  |  |
|  | 9 | Finish Lang OV II Soln to PS1 and 2 |  |  |  |  |
|  | 10 | Lang OV III to slide 22 PS4 | PS4 | W 9/24 |  |  |
| M | 11 | Finish Laguage OV III - Attributes |  |  |  |  |
|  | 12 | PS 5 Low class attendance due to career fair | PS5 | M 9/29 |  |  |
|  | 13 | Timing and Concurrency I |  |  |  |  |
| M | 14 | Timing and Concurrency II thru slide 15 | PS6 | F 10/3 |  |  |
|  | 15 | Timing and Concurreny **III thru slide 23**  | **OCT 1** |  |  |  |
|  | 16 | **Resolution through 17** |  |  |  |  |
| M | 17 | Floating Point PS 7 – register set | PS7 | F 10/10 |  |  |
|  | 18 | At NSF |  |  |  |  |
|  | 19 | Floating Point | PS10 | W10/22 |  |  |
| M | 20 | PS 10 - shared libraries |  |  |  |  |
|  | 21 | PS8 – integrating registers with dp | PS8 | W10/22 |  |  |
|  | 22 | On travel |  |  |  |  |
| M | 23 | On travel |  |  |  |  |
|  | 24 | On travel |  |  |  |  |
|  | 25 | Cleanup – Sequential logic modeling | PS 9 |  |  |  |
|  |  |  | **NOV** |  |  |  |
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