Spring 2016 ECE 3561 Advanced Digital Design

Material Covered

|  |  |  |  |  |  |
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| **C** | **D** | **Topic** | **Assign** | **Due** |  |
| *1* | M | Jan 11- Lecture 1 - Intro |  |  |  |
| 2 |  | Lect 2 – Digital Logic Basics | Prob 11.1 |  |  |
| 3 |  | Lect 3 – Common Elements in Sequential Design | none |  |  |
| 4 | W | Jan 20 Lect 5 – Sequential Circuit Design – Traditional | See web page |  |  |
| 5 |  | Lect 6 – State Graphs and State Tbls thru slide 14 |  |  | Quiz 1 |
| 6 | M | Jan 25 – Lect 7 – Moore |  |  |  |
| 7 |  |  Lect 7s – Multiple output |  |  |  |
| 8 |  | San Diego – CEAA |  |  |  |
| 9 | M | Feb 1 – Lect 8 – State Tbl Reduction thru slide 23 |  |  |  |
| 10 |  | Open session due to career fair |  |  |  |
| 11 |  | Lect 9 – State Assignment |  |  | Quiz 2 |
| 12 | M | Feb 8 AT NSF |  |  |  |
| 13 |  | Finish L9 - finish |  |  |  |
| 14 |  | Lect 10 Quiz  |  |  | Quiz 3 |
| 15 | M | Feb 15 Finish L10 one hot Lect 10 a  |  |  |  |
| 16 |  | L11 - State Machine Analysis from 10 Problem working session |  |  |  |
| 17 |  | VHDL Overview to slide 16 | VHDL 1 | Feb 24 | Quiz 4 |
| 18 | M | Feb 22 – VHDL Language Elements |  |  |  |
| 19 |  | VHDL Language Elements II |  |  |  |
| 20 |  | Exam Review |  |  |  |
| 21 | M | Feb 29 – DVCON **Midterm** |  |  |  |
| 22 |  | Mar 2  |  |  |  |
| 23 |  | Mar 4 – VHDL Spec of State Mach |  |  |  |
| 24 | M | Mar 7 At NSF |  |  |  |
| 25 |  |  |  |  |  |
| 26 |  |  |  |  |  |
|  | M | SPRING BREAK |  |  |  |
| 27 | M | Mar 21 |  |  |  |
| 28 |  |  |  |  |  |
| 29 |  |  |  |  |  |
| 30 | M | Mar 28 |  |  |  |
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| 32 |  |  |  |  |  |
| 33 | M | Apr 4 |  |  |  |
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| 36 | M | Apr 11 |  |  |  |
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| 39 | M | Apr 18 |  |  |  |
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| 42 | M | Apr 25 Last Day |  |  |  |
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