SPRING 2014

Material Covered

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| L | D | Topic | Assgn | Due |
| 1 | M | Lect 1 – Overview – only covered syllabus and to slide 5 due to championship game |  |  |
| 2 | W | Finish Lect 1 and Lect 2 to slide 22 | Read 11, P 11.1 |  |
| 3 | F | Finish Lect 2 - Lect 3 | VHDL Assgn 1 | Wed Jan 21 |
| 4 | W | Cover using Modelsim and Quartis | Comp Assgn 1 |  |
| 5 | F | No class – IEEE CEAA New Orleans |  |  |
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Spring 2014

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| L | D | Topic | Assgn | Due |
|  | **M** | Weather Day |  |  |
| 1 | W | Lecture 1 - Intro | None |  |
| 2 | F | L2 – Sequential Design Basics | 11.1 x | --- |
| 3 | **M** | Go over 11.1 - L3 – Memory Elements – Registers Finished thru slide 11 |  |  |
| 4 | W | Present PR1 – finish L3 – L4 – Quartis OV | Project 1 | Jan 22 to PR1 |
|  | F | IEEE CEAA meeting in San Diego |  |  |
|  | M | Holiday |  |  |
| 5 | **W** | L5 – Sequential circ design thru 5 |  |  |
| 6 | F | L5 - finish | HW2 | Jan 31 to HW2 |
| 7 | **M** | L6 – State Graphs and Tables | Prog ex 14.1 | Not for turn in |
| 8 | W | L7 – State Graphs and Tables – Moore Mach | PE 14.12, 14.4 | Not for turn in |
| 11 | F | L8 – State Reduction | 14.26 enumerated | Drop Box HW3 – Feb 3 |
| 12 | **M** | Lect 12 – VHDL overview – review 14.26  Through slide 6 |  |  |
| 13 | W | Open discussion |  |  |
| 14 | F | Lect 13 – VHDL Language Elements 1 |  |  |
| 15 | **M** | Nsf – Feb 10 |  |  |
| 16 | W | VHDLL13 lang Elements 1 thru slide 15 |  |  |
| 17 | F | VHDL L13 Lang Elements I to end | Sem Proj 2  4-to-1 mux syn | Due Wed Feb 19 |
| 18 | **M** | VHDL L14 Lang Elements II Spec of State Mach thru slide 9 |  |  |
| 19 | W | (Feb19) Finish L14 Lect 15 thru 10 |  |  |
| 20 | F | Demo of Model Sim – Semester Proj a3 | Sem Proj 3  4-to-1 sim | Due Fri Feb 28 |
| 21 | M | (2/24) Finish L15 – Lect 16 Testbenches SM |  |  |
| 22 | W | Sem proj a4 - L17 – VHDL SM bin states |  |  |
| 23 | F | Live demo of Modelsim and Quartus Exam Review |  |  |
| 24 | M | At DVCON - Midterm |  |  |
| 25 | W | Work on project |  |  |
| 26 | F | Work on project **SPRING BREAK** |  |  |
| 27 | M | Time change messup |  |  |
| 28 | W | Exam return/ Exam review |  |  |
| 29 | F | Project discussion |  |  |
| 30 | M | Lect 18 – VHDL for other |  |  |
| 31 | W | Lect 19 – Resolved signals |  |  |
| 32 | F | Lect 20 – Register Set |  |  |
| 33 | M | Lect 21 – Register Set Testing |  |  |
| 34 | W | Lect 22 – Debugging the register set |  |  |
| 35 | F |  |  |  |