SP a 8: Semester Project assignment 8

In this step the register set will be created for the datapath.

The register set output is capable of driving

There will be 16 registers, each of which is as shown below. Not that you also have to add the address decoder for the input and separate address decoders/drive units for generating the drvAx and drvBx signals



If possible a testbench will be provided to test this unit. At the next higher level it looks like:



Also, synthesize it and include the synthesis result in your report.

An updated view of the register structure is below. This structure is repeated 16 times for a 16 bit register set. Register 0 is shown.



At the top level the unit will have an interface that looks like this.



There is also a testbench tbdp4.vhdl that is a modification of tbalu3.vhdl. The modification is to include the signals that drive the register set.

The timing of all signals to include the registers is below.

