SP a 7: Semester Project assignment 7

Take you code from step a6 and add input registers that latch in type std\_logic\_vector and use type conversion to have output of bit\_vector.

Add the output bus driver which will take as input the bit\_vector output of the ALU and drive the std\_logic\_vector bus. Also, off of the bit vector output the n, negative and z, zero flags are generated.

A diagram of the unit looks like:



Simulate this unit, write a report and submit it to the dropbox for SP a7.

Also, synthesize it and include the synthesis result in your report.