SP a 5: Semester Project assignment 5

This is another step in the semester project. This part of the project will be simply writing VHDL code for several new units.

They are

A 16-bit bus driver

A 16-bit register unit

A 4-to-16 de-multiplexer – THIS UNIT NEEDS TO BE TESTED so write a testbench and do a simulation that exhaustively runs through the 16 input cases.