SP a 1: Semester Project assignment 3

This is another step in the semester project. This part of the project will be construction, HDL modeling, HDL simulation, and synthesis of the core of the ALU. The first step was coding and synthesis of the logic unit.

Note that these are 16 bit operational units. For the logic operations they are accomplished by a 4-to-1 multiplexor. The assignment was for one bit of the 16 for the logic unit. Use the generate statement or straight component instantiation to extend it into a 16-bit unit. This can be built hierarchically: ENTITY and ARCHITECTURE for a 1-bit 4-to-1 mux, ENTITY and ARCHITECTURE for the 16-bit logic unit which uses the 4-to-1 mux.



Also model the arithmetic unit as 16-bit. This can be done by creating an ENTITY and ARCHITECTURE for a full adder. Then a 16-bit unit ENTITY and ARCHITECTURE is created by using that full adder 16 times.

Write a testbench to test your 16-bit logic unit and your 16-bit adder unit. If you have exhaustively tested the 1-bit version then the 16-bit versions just need tests to confirm that the implementation was wired up correctly. For the Logic Unit a few logic operations on a couple of A and B inputs, well chosen, should do. The same is true for the Arithmetic Unit. Here you will need to make sure the carry can ripple from the carry in to the carry out. There is a shell for an exhaustive testbench for the 16 bit adder. I don’t actually recommend using it as it take a long while to execute as 2^32 vectors would need to be applied for cin=0 and cin=1. This is way too much data without automatic error checking and not really needed.

Then combine these two units with a 16-bit 2-to-1 multiplexor.

For turn in: You will need to turn in all the ENTITY ARCHITECTURE models for all units and the results of all Model Sim simulations by submitting the appropriate waveforms. There should be a waveform for the 1-bit logic cell and the 16-bit logic unit, the 1 bit full adder and the 16-bit adder.

Then onto Quartus. Create a new project as the first will be synthesis of the 16-bit logic unit. The next will be synthesis of the 16-bit arithmetic unit. And finally synthesis of this core of the ALU. For each create a report showing the number of combination LUTs, F/Fs (which should be none), and the schematic(s).

When using Quartus for either 16 bit unit, use the VHDL ENTITY ARCHITECTURE for the 1 bit unit and also use the structural 16-bit ENTITY ARCHITECTUE.