SP a 1: Semester Project assignment 3

This is the first coding step in the semester project. The part of the project is the testing of the logic unit for the ALU model of the microcontroller. The first step was coding and synthesis of the logic unit. Now to logically test it.

Note that these are 16 bit operational units. For the logic operations they are accomplished by a 4-to-1 multiplexor. The assignment was for one bit of the 16 for the logic unit. This is testing before that unit is made into a 16-bit unit.



This assignment is to take the VHDL model of the 4-to-1 multiplexor that you wrote, link it into the testbench in file Logic\_Unit.vhdl, and then simulate using ModelSim.

INPUTS: A, B, C0, C1, C2, C3

OUTPUT: R

R = A’B’C0 + A’B C1 + A B’ C2 + A B C3 (The logic equation for a 4-to-1 mux)

Go to one of the department PCs or workstations and boot up Modelsim. Create a Library work for storing your design units. Then compile your model into it. Also compile in the testbench after you finish its code.