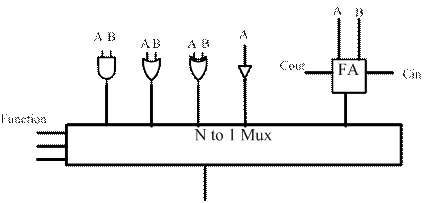
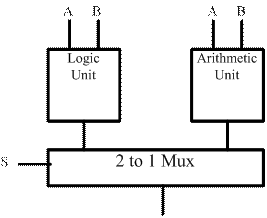
SP a 1: Semester Project assignment 2

This is the first coding step in the semester project. The part of the project is the design of the logic unit for the ALU model of the microcontroller. There are two possible approaches to it. The first is a brute force approach where you have units to do each operation and then multiplex the correct one out for the logic operation.



The second approach is to have a unit to do logic operations and an efficient adder for addition and subtraction. Note that these are 16 bit operational units. For the logic operations they are accomplished by a 4-to-1 multiplexor.



This assignment is to write a VHDL model of a 4-to-1 multiplexor.

INPUTS: A, B, C0, C1, C2, C3

OUTPUT: R

R = A’B’C0 + A’B C1 + A B’ C2 + A B C3 (The logic equation for a 4-to-1 mux)

The VHLD description will have the 6 inputs as type BIT and one output also type BIT.

These will be in the PORT list in the ENTITY.

The logic equation goes in the architecture which just contains that 1 statement.

Once your create a text file of this synthesize it in Quartis. Screen capture after, and specifically note the number of CLB it took to implement this unit.