This document explains the code and the testbench of alu1.

A diagram of the alu1 architecture is shown in Figure 1:



Figure 1. alu1 architecture

The code has been created structurally and is in files (list files)

To test this a simple testbench is written that instantiates the component and then applies tests.

There are 6 fixed input vectors.

First these vectors will be applied to the logic unit to test the logic operations of AND, OR, XOR, Invert A, and Zero.

Look at the testbench which applies the tests linearly and had about 175 lines of code.

Now on to the Quartis and synthesis of the unit.

Creating an alu1 project and including the VHDL files results in the following synthesis of the unit.



If you double click on the lu16 unit you now have the following schematic.

 

And for the output multiplexor have the following:

 

You can repeat this on the adder unit



And decending



Interesting to note the symbol for a 3 input XOR gate.

These result are as expected.

How many FPGA resources are used?

Logic Utilization

Combinational LUTs – 40

Total Pins

55

NO REGISTERS??? You would expect no register as this is a completely combinational design.