This assignment is to create the microbaby Arithmetic Logic Unit (ALU). The ALU will be constructed from components in VHDL and tested with a testbench using ModelSIM. The testbench will be provided and is talu. After creating a structural architecture of the ALU (structural except for a signal assignment statement to create bbar, bbar <= not b), text it using the provided testbench. After the VHDL simulation is done, synthesize the ALU using QUARTIS.

The components are:

2-to-1 mux – was done for you here as an example of what is to be done

2-to-1x8 mux - was done for you here as an example of what is to be done

1-bit register

* 4-to-1 mux (model it with a single concurrent signal assignment statement similar to the one used for the 2-to-1 mux.
* 4-to-1x8 mux (by multiplexing bit vectors via a selected or conditional signal assignment, not by use a single bit mux)
* All 0’s detector for testing an 8-bit byte to see if it is all 0’s
* full\_adder
* 8-bit adder constructed from 8 instantiations of the full adder
* 8-bit register constructed from 8 instantiations of a 1-bit register
* 8-bit Bus Driver

For the Report the format is much the same except that the only VHDL submitted is the MBALU.VHDL code.

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Your name and name.1 Component name

**HDL CODE of the ALU**

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

ENTITY mbalu IS

 PORT (lots of signals);

END mbalu;

ARCHITECTURE one OF mbalu IS

 --Component declarations and configurations

 --Any internal signals to connect things up

BEGIN

 --structural architecture

END one;

**SIMULATION RESULTS**

Simulation done on testbench with resolution set to ns.

Signals display are all object in testbench region

Could be done by Fn-Print Screen capture



Or highlighting the simulation window and then using export and getting a bitmap image (preferred)



**The Quartis Synthesis**

The code is put into Quartis and the following results are obtained:

Basic information

Combination ALUTs 1

Registers 0

Pins 4

RTL viewer



**END OF REPORT**

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