8-bit register

An 8 bit register is needed for the accumulator and for holding the B-input. The unit has the following high level look:



Inputs: Din : STD\_LOGIC\_VECTOR (7 downto 0)

Load : STD\_LOGIC --the load occurs on a rising transition of the signal

Output : Dout : STD\_LOGIC\_VECTOR (7 downto 0)

* **Write the VHDL ENTITY and ARCHITECTURE code for this 8-bit register.** Don’t forget to use the LIBRARY and USE clause for using std\_logic.
* **Modify an earlier testbench to test this architecture.** It will also need the LIBRARY and USE clause for using std\_logic. The testbench needed is not extensive. Load values of “11111111”, “00000000” and “01010101” into the register and you are done.
* **Synthesize the design using Quartis**

In your report be sure to show the circuit synthesized by Quartis ala the sample report.

Submit it to the dropbox MB Comp 9.