This assignment continues the process of building up the components of the datapath of Microbaby.

This assignment is very similar to MB Comp 2. In that assignment the 4-to-1 muxtiplexer was used to generate an eight bit version where there are 8 connections for each of the 4 data inputs (TYPE BIT\_VECTOR(7 downto 0)). There are 2 select inputs that connect to all 8 instantiations.

In this assignment the 4-to-1 mux will be laid on its side and each of the data inputs is connected to each of the 8 instances. For the other 2 inputs (the selects) there will be a connection to an input. It will be of type bit vector.

The entity will be as follows:

ENTITY one OF lu IS -- lu stands for logic unit.

 PORT (FUNC : IN BIT\_VECTOR (3 downto 0);

 A,B : IN BIT+VECTOR(8 downto 0);

 R : OUT BIT\_VECTOR(8 downto 0));

END one;

The structure of the unit is capable of generating any logic function on the A and B inputs by inputting the truth table of the logic function on FUNC. For example, for an AND function, FUNC would be set to “1000”, for an OR function, FUNC would be set to “1110”.



Compile your VHDL code. Modify the testbench of the ha and fa to test your code and simulate so that all cases are simulated. Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the sample report.

Submit it to the dropbox.