In the MB Comp 5 assignment an 8-bit full adder was designed. This was a ripple carry adder. In this assignment it will be contrasted against a carry select adder.

The architecture is shown in the figure below



Figure 1. 8-bit Carry Select Adder

To implement this write a VHDL ENTITY and ARCHITECTURE for a 4-bit adder and a 4-bit 2-to-1 muxtiplexer. You can use the single bit 2-to-1 mux you already have. Combine these units structurally into the architecture depicted above. Note the sum for bits 7 downto 4 are the output of the 4-bit 2-to-1 mux.

Write the VHLD and instantiate it into the full adder testbench as second architecture to be tested. Simulate it and the output of the two adders should be identical.

Include the code for this new adder in the report along with simulation results.

Now synthesize this unit using Quartis. After doing the synthesis, place and route the design. After the place and route you can do a Circuit timing analysis. Look at the report and you will find it reports the time for the longest path. For the 1-bit full adder, fa, it was a to cout and was 9.96 ns. Do this analysis for both the ripple carry 8-bit adder and the 8-bit carry select. For the 8-bit adders, the maximum time should be from a(0) or b(0) or cin to cout. Note this in your report and provide comment on the times.

Be sure to have headers or comment that identifies the figure that is being presented.