This assignment starts the process of building up the components of the datapath of Microbaby.

In this assignment you will use VHDL.

Using the ENTITY and an ARCHITECTURE (dataflow) of a 2-to-1 muxtiplexer, structurally build it up into an 8 bit unit.

There is 1 select inputs, sel 0. There are 2 data inputs D1,D2 each of which is type BIT\_VECTOR (7 downto 0). You can access each element of the inputs using D1(0) to specify the rightmost bit of the vector D1

There is one output,z,which is also a BIT\_VECTOR of the same size.

Use type BIT and BIT\_VECTOR.

Compile your VHDL code. Modify the testbench of the ha and fa to test your code and simulate so that all cases are simulated. Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the sample report.

Submit it to the dropbox.