This assignment starts the process of building up the components of the datapath of Microbaby.

In this assignment you will use VHDL.

Write an ENTITY and an ARCHITECTURE (dataflow) of a 2-to-1 muxtiplexer.

There is 1 select inputs sel 0. There are 2 data inputs D1 and D2.

There is one output,z,which performs per the table below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Sel0** |  | **Out z** |  |
|  | 0 |  | D1 |  |
|  | 1 |  | D2 |  |

Use type BIT for the input and output.

Compile your VHDL code. Modify the testbench of the ha and fa to test your code and simulate so that all cases are simulated. Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the sample report.

Submit it to the dropbox.