The CPU

 The ALU just finished in MB Comp 10 will be integrated with a few other components to form the Central Processing Unit (CPU) of the MicroBaby processor. This structure is shown below:



The MicroBaby CPU

InOut DataBus : STD\_LOGIC\_VECTOR (7 downto 0)

Inputs: DrAcc : STD\_LOGIC --When DrAcc is asserted high, the DataBus is driven to the

 value of the Accumulator. When DrAcc is not high,

 DataBus is given the value “ZZZZZZZZ”

 BmuxLatch : STD\_LOGIC --on a rising edge transition the output of bmux is latched

 Aal : STD\_LOGIC --select signal that selects the input to the accumulator

 Bbu : STD\_LOGIC --select a fixed “00000000” or the DataBus

 Ldac : STD\_LOGIC --load the accumulator on the rising edge

 The remainder of the signals are those for the ALU and are type BIT and BIT\_VECTOR Refer to the ALU assignment for their definition.

The timing associated with the bus is a 100 ns cycle. Watching the simulation run shows the application of the control signals as controlled by the test bench. A sample of the waveform of the simulation is at the end of this description.

An 8-bit 2to1mux will be needed that uses STD\_LOGIC\_VECTOR. Call it mux2\_1x8r perhaps.

* **Using the shell provided complete the VHDL ENTITY and ARCHITECTURE code for CPU.** This will only involve component declarations, configurations and instantiations. The type conversion functions are included in the file.
* **The testbench is provided as it more involved.** It will also need the LIBRARY and USE clause for using std\_logic. The testbench needed is not extensive. Drives values of “11111111”, “00000000” and “01010101” to the output. Be sure to separate these drive periods by a period where you are not diving the output to show that the output goes to high-impedance.
* **Synthesize the design using Quartis**

In your report be sure to show the circuit synthesized by Quartis ala the sample report. Also be sure to show the expanded waveform that shows clearly each operation through simulation. When you do the synthesis make sure you have all of the component hierarchy in the directory.

Submit it to the dropbox MB Comp 9.

The files included here are

tbc.vhdl The test bench for MicroBaby CPU component.

mbcpu\_shell.vhdl The VHDL shell for the mbcpu unit. You need to add component declarations and configurations along with their instantiations. The type conversion functions are provided.

mbpcu.do This is a .do file to set up the waveform display during simulation. The waveform shown here uses this format file. This is the result when a Simulate->Run-All is selected.

