MicroBaby Datapath Component.

The MicroBaby data path can now be built up from the MB ALU, registers, multiplexers, and a bus driver. It has the following look:



VHDL Part:

Write the ENTITY and an ARCHITECTURE of structural architecture of the MicroBaby datapath.

All Inputs and Outputs are of type std\_logic or std\_logic\_vector.

Compile your VHDL code. Modify a testbench (probably from the ALU) to test your code and simulate. Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the report online for the mux\_2to1.

Submit it to the dropbox mb6.