MicroBaby Datapath Component.

The MicroBaby data path has only one new component not modeled so far, a bus driver. That is the unit to be modeled here.

The bus driver has the following look:



The data input is driven onto the BUS whenever DrBus is asserted (a ‘1’) and when not asserted BUS is high impedance.

This can be accomplished in VHDL using a SELECTED or CONDITIONAL signal assignment statement. The CONDITIONAL form would be

 BUS <= Data WHEN DrBus=’1’ ELSE “ZZZZ…Z”;

where the number of Z’s in the vector conforms to the size of Data and the BUS. BUS is a reserved word in VHDL so use your name for the data bus of MicroBaby.

VHDL Part:

Write the ENTITY and an ARCHITECTURE of the bus driver.

Data Inputs and BUS are of type std\_logic\_vector(7 downto 0).

Compile your VHDL code. Modify a testbench to test your code and simulate. Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the report online for the mux\_2to1.

Submit it to the dropbox mb8.