Component 7 of the MicroBaby Architecture is the ALU of the data path. It will piece together the components we have created so far. The diagram below depicts the ALU architecture. (2x points)



The unit has INPUTS:

A, B 8-bit std\_logic\_vector

AddSub std\_logic and indicates if an add (0) or subtract (1) is to be performed

Cin std\_logic The carry in

Csel std\_logic\_vector (2-btis) controlling the 4-to-1 mux selecting the cin to the adder

Arlo std\_logic control signal that specifies if an arithmetic or logic operation

The unit has the following OUTPUTS

Res 8-bit std\_logic\_vector the is the output of the operation

Cout std\_logic that is the carry output

N std\_logic and is the negative flag (msb of Res)

Z std\_logic and is the zero flag – value of 1 if Res is all 0’s

VHDL Part:

Write the ENTITY and an ARCHITECTURE for this unit. It will only use component instantiations. The only concurrent signal assignment statement is Bbar <= NOT B; to generate the complement of B needed for one input to the 2-to-1 x 8-bit multiplexer.

Compile your VHDL code. Modify a testbench to test your code and simulate or use the testbench that will be on the webpage for testing the unit.. Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. You will need a copy of the VHDL code for all the components used in the structural architecture along with the structural code for the ALU architecture.

In the report you create when you are generating the schematic of the components include the top level and the structure for each of the components in it. Go down into the architecture until you reach primitives.

Submit it to the dropbox mb7.