Another of the components of the datapath of Microbaby is an 8-bit adder. This adder will implement a carry select added with two 4-bit stages. The 1st 4-bit stage is just a standard ripple carry adder with the initial carry in. It generates the 4 lsb of the output and a carry out that is used for selecting the correct option for the 2nd stage. In this stage the upper 4-bit adder has a presumed 0 carry in and the lower has a presumed carry 1 in. The initial stage carry output is used to control a multiplexer that chooses the correct one.

VHDL Part:

Write the ENTITY and an ARCHITECTURE of a 8-bit all 2 stage carry select adder..

Inputs and Outputs are of type std\_logic\_vector.

Compile your VHDL code. Modify a testbench to test your code and simulate. Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the report online for the mux\_2to1.

Submit it to the dropbox mb6.