Another of the components of the datapath of Microbaby is an 8-bit all 0s detector. This unit has and 8-bit input and generates an output, all0 = ‘1’, when all 8 bits of the byte are ‘0’. This is simply a nor of all 8 bits.

VHDL Part:

Write the ENTITY and an ARCHITECTURE of a 8-bit all 0s detector.

In the ARCHITECTURE, model this unit using a single concurrent signal assignment statement.

The input is the 8-bit byte as a bit\_vector. The output is a single bit, type std\_logic.

Compile your VHDL code. Modify a testbench to test your code and simulate so that all cases are simulated (not much is needed to test the unit). Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the report online for the mux\_2to1.

Submit it to the dropbox mb5.