Another of the components of the datapath of Microbaby is an 8-bit register. We have seen the code for registers when doing state machines.

VHDL Part:

Write the ENTITY and an ARCHITECTURE of a 8-bit register, reg8.

In the ARCHITECTURE, model this unit as registers were modeled in the state machines.

There is 1-bit input latch which causes latching of data\_in into the register on the rising edge.

The output data\_out is the value of the contents in the register.

Compile your VHDL code. Modify a testbench to test your code and simulate so that all cases are simulated (not much is needed to test the unit). Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the report online for the mux\_2to1.

Submit it to the dropbox mb4.