Another of the components of the datapath of Microbaby is an 8-bit word 4-to-1 muxliplexer. This unit will be used as the logic operation unit within the ALU. There is a VHDL part to the assignment and a Quartis part to the assignment.

VHDL Part:

Write the ENTITY and an ARCHITECTURE of a 4-to-1 by 8-bit muxtiplexer, mux4\_1x8.

In the ARCHITECTURE you can model this unit structurally using your 4-to-1 mux component or write a dataflow architecture. In synthesis you should get the same results.

There is 1 select inputs, sel which is a vector 1 downto 0. There are 4 data inputs, D0 to D3 each of which is type std\_logic\_vector (7 downto 0). You can access each element of the inputs using D1(0) to specify the rightmost bit of the vector D1

There is one output, z, which is also a std\_logic\_vector of the same size.

Suggestion: Use a conditional or selected signal assignment statement.

Compile your VHDL code. Modify the testbench of the ha and fa to test your code and simulate so that all cases are simulated (not much is needed to test the unit). Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the report online for the mux\_2to1.

Submit it to the dropbox mb3.