Another of the components of the datapath of Microbaby is a 4-to-1 muxliplexer. There is VHDL part to the assignment and a Quartis part to the assignment.

VHDL Part:

Write the ENTITY and an ARCHITECTURE of a 4-to-1 muxtiplexer, mux\_4to1.

There is 1 select inputs which is 2 bits, sel (1 downto 0). There are 4 data inputs, D0, D1, D2 and D3, each of which is type std\_logic. You can access each element of the inputs using its signal name.

There is one output, z, which is also of type std\_logic.

Compile your VHDL code. Modify a testbench to test your code and simulate so that all cases are simulated (not much is needed to test the unit). Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the report online for the mux\_2to1.

Submit it to the dropbox mb2.