Integration with conroller.

The MicroBaby architecture is the hookup of the datapath to the controller and memory to form the processor.



VHDL Part:

Here you can hook your datapath into the supplied model to see it simulate with the remainder of the components.

All Inputs and Outputs are of type std\_logic or std\_logic\_vector.

Compile your VHDL code. Modify a testbench (probably from the ALU) to test your code and simulate. Prepare a report showing your VHDL results.

Submit it to the dropbox mb10.