This assignment starts the process of building up the components of the datapath of Microbaby. A design of a mux\_2to1 can be found on the web page and can be downloaded. The 8-bit version could be created structurally from connecting up 8 of the single element ones, however, the intent is to use and 8-bit std\_logic\_vector.

In this assignment you will use VHDL.

Using the ENTITY and an ARCHITECTURE of a 2-to-1 muxtiplexer, modify it to make it into an 8 bit unit.

There is 1 select inputs, sel 0. There are 2 data inputs, D1 and D2, each of which is type std\_logic\_vector (7 downto 0). You can access each element of the inputs using D1(0) to specify the rightmost bit of the vector D1

There is one output, z, which is also a std\_logic\_vector of the same size.

Suggestion: Use a conditional or selected signal assignment statement.

Compile your VHDL code. Modify the testbench of the ha and fa to test your code and simulate so that all cases are simulated (not much is needed to test the unit). Prepare a report showing your VHDL results.

Start up Quartis and perform a synthesis on your design. In your report be sure to show the circuit synthesized by Quartis ala the report online for the mux\_2to1.

Submit it to the dropbox mb1.