**VHDL Assignment #2 – HW 7**

In this assignment you will be creating a VHDL state machine description for the sequence detector from Lecture 6. This is the machine that will detect input sequences that end in 010 or 1001. The state machine is shown here. There is one input X and an output Z.



Follow the state machine description methodology shown in class.

Write a VHDL description for this state machine using the 3 process methodology discussed.

Note that this is a Mealy machine and part of the VHDL is done for you.

The testbench and code framework is in file vass2.vhdl and can be downloaded.

Once you have your code completed, compile it in ModelSim.

The testbench has a test stream that tests your design.

**Report Format for turn in:**

Create a word document that contains the following:

The VHDL code

The Waveform for the complete simulation that shows X,clk,Z, the state of the state machine