**VHDL Assignment #6 – vass6**

This one is VHDL and synthesis of Example 1 in section 14.3 of the text: “A sequential circuit has one input (X) and one output (Z). The circuit examines groups of four consecutive inputs and produces an output Z = 1 if the input sequence 0101 or 1001 occurs. The circuit resets after every four inputs. Find the Mealy state graph.”

This problem is solved in the test to give you the state graph. Implement the state graph in VHDL and simulate. Once again you can use the setup code of vass4 changing names to vass6.vhdl and ENTITY vass6 IS …. Etc. You may also need to edit the x\_sequence to test that is has the cases you need.

Create a .docx report that includes the code that the results of simulation that clearly shows the results.

Start Quartis and synthesize the units. Add to it the information on the resources used, the diagram of what was synthesized, and the state machine diagram.

Now resynthesize the uni,t only this time force it to do a one-hot encoding. Comment on the resources needed (LUTs and F/Fs) and the diagrams available in the reports.