**VHDL Assignment #4 – vass4**

In this assignment you will be doing creating a state machine description for a sequence detector that detects the input sequence ending in 101.

The state machine has a single input X and a single output Z that is 1 when the sequence is detected.

Implement this for both a Mealy and Moore machine. Create the state diagrams (can be found in slides).

Create a VHDL model and simulate both models (same entity, different architectures) in the same testbench for an input sequence that tests the designs. Create a .docx report that includes the code that the results of simulation that clearly show the results.

Start Quartis and synthesize the units. Add to it the information on the resources used, the diagram of what was synthesized, and the state machine diagram.