**VHDL Assignment #3 – HW 9**

In this assignment you will be doing creating a state machine description for a 3-bit counter that counts 0 to 7. In the first version you will use symbolic state names s0, s1, … , s7. In the second you will use binary encoding 000, 001, 010, … , 111.

Follow the state machine description methodology shown in class. A testbench is provided as is the entity for the state machine.

The ENTITY for the state machine is:

 ENTITY cntr3 IS

 PORT (clk : IN BIT;

 cnt : OUT BIT\_VECTOR (2 downto 0));

 END cnt3;

Note that in the version where the states are represented symbolically you will need an output process to assign the output values to signal cnt which has a CASE statement and assigns the value based upon the state. In the case of the binary encoded states you will simply directly assign the current state (signal state) to the output cnt using a concurrent signal assignment statement.

Both write the VHDL code, test the VHDL code, and the Synthesize the code in Quartis.