**VHDL Assignment #2 – HW 7**

In this assignment you will be doing creating a state machine description for the sequence detector from Lecture 6. This is the machine that will detect input sequences that end in 010 or 1001. The state machine is shown here. There is one input X and an output Z.

Follow the state machine description methodology shown in class.

Write a VHDL description for this state machine using the 3 process methodology discussed.

Note that this is a Mealy machine.

Once you have your code completed, compile it in ModelSim.

Write a testbench and instantiate it into the testbench.

Create a test stream that tests your design.

**HW8 –** Create a project in Quartis and synthesize this design into an FPGA implementation.

In a report (word document) show the schematic of the machine generated and the reports that shows the number of F/F and LUTs used.