NAME: _____

THIS IS AN "Take Home" EXAM. As such you have access to reference material, electronic textbook/notes – OK. Help from anyone, except the TA or the instructor, is considered a violation of the honor code and not allowed.

1. (30 points) Generate a MEALY Machine with the following specification.
The sequential machine has a single input X and a single output Z.
The machine detects input sequences ending in 0101 and the output Z = 1 when the sequence is detected. Z = 0 otherwise.

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INPUT     0 0 0 1 0 0 1 0 1 0 1 0 0 1 0 1 1 1 0 1 0 1 1
OUTPUT    0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 1 0 0 0 0 0 1 0
```

(10) A) Create a state machine diagram for this machine and ensure it is minimal. The work to do this can be done on paper, but will be scanned and pasted into the doc file for this problem.
(10) B) Create a VHDL file for this state machine that has an ENTITY and ARCHITECTURE. The ENTITY will have X,Z, and CLK in the port list and they will be type BIT; The ARCHITECTURE will contain the three processes for modeling a state machine, the first to latch next_state to state, the second for the generation of next state using a case statement, and the third for generation of the output. In the declarative region declare an enumeration type for the states symbolically as s0,s1,s2, etc.
C) The simulation of this state machine with be combined with the simulation of the state machine of problem 2. In problem 3. In simulation the output is tied to Zmealy.
(10) D) Synthesize the state machine using QUARTIS. Include the following in your report. The number of LUTs and registers required. Also include the RTL viewer circuit generated and the state machine view. (Both the circuit and the state machine)

REPORT REQUIREMENT:
A) STATE DIAGRAM Development : state diagram, implication table (scanned and pasted in)
B) VHDL CODE OF STATE MACHINE
D) SYNTHESIS RESULTS

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2. (30 points) Generate a MOORE Machine with the following specification.
The sequential machine has a single input X and a single output Z.
The machine detects input sequences ending in 0101 and the output Z = 1 when the sequence is detected. Z = 0 otherwise.

(10) A) Create a state machine diagram for this machine and ensure it is minimal. The work to do this can be done on paper, but will be scanned and pasted into the doc file for this problem.

(10) B) Create a VHDL file for this state machine that has an ENTITY and ARCHITECTURE. The ENTITY will have X,Z, and CLK in the port list and they will be type BIT; The ARCHITECTURE will contain the three processes for modeling a state machine, the first to latch next_state to state, the second for the generation of next state using a case statement, and the third for generation of the output. In the declarative region declare an enumeration type for the states symbolically as s0,s1,s2, etc.
C) The simulation of this state machine with be combined with the simulation of the state machine of problem 2 in problem 3. In simulation the output is tied to Zmoore.
(10) D) Synthesize the state machine using QUARTIS. Include the following in your report. The number of LUTs and registers required. Also include the RTL viewer circuit generated and the state machine view. Both the circuit and state machine.

REPORT REQUIREMENT are the same as for 1

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3. (20 points) VHDL SIMULATION

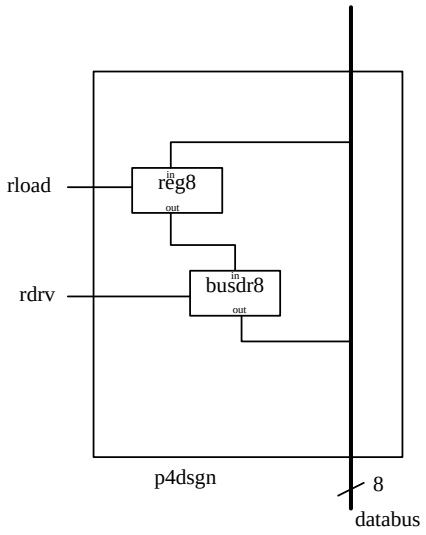
Simulate the architectures of 1 and 2 using the testbench provided. Run the simulation. You cannot use run all as there is a clock and the testbench never goes quiescent. Run it for until all inputs are exhausted (400 ns should do it).

REPORT REQUIREMENT
As your code is included in 1 and 2 you do not need to include it here. Just include the simulation results and a one or two sentence comment on what is shown in the simulation (5).

4. (20 points) Using std_logci

Create a VHDL model that instantiates an 8-bit Register and an 8-bit Bus Driver.
The ENTITY of the model will contain a std_logic_vector (7 downto 0) signal for data_bus, and std_logic control signals for rload, rdrv.
The models for the register and bus_driver can be ones that you have or develop for the exam.

For the p4dsgn.vhdl they need to be declared, configured, and then instantiated as appropriate.
Declare any local signal that you need. The unit will be configured as shown in the figure below.



p4dsgn.vhdl will tested using the testbench provided. It will run through several bus cycles transferring data to the register and then driving the register back onto the bus.

For the waveform, show the signal xxx, yyy from the testbench as the internal signal used to connect the output of the register to the input of the bus driver in p4dsgn.vhdl.

P4 REPORT

(5) Register VHDL code

(5) Bus Driver VHDL code

(5) P4dsgn.vhld code

Code of the **testbench tp4** with p4dsgn declared, configured and instantiated.

(5) Copy of the **waveform**. This design can be run using run all and there is not a free running clock.

You do not have to use QUARTIS on this design.