In this assignment you will be implementing the complete DATA Path of microbaby.

Having the various components (all using TYPE std\_logic), it is time to put the Data Path of Microbaby together. You should have an ALU from your previous or you can use the ALU on the webpage.

The Datra Path has the following structure.



The large component is the ALU. There are also 2 2-to-1x8-bit multiplexers. You already have this component.

A new component is an 8-bit register with a load signal, data in and data out.

A second new component is an 8-bit bus driver. When drive is asserted (high) then the output goes to the value of the input. Otherwise it is high impedance, Z.

The control signals of the interface of the datapath:

INPUTS

A,B – 8-bit std\_logic\_vector

Cin – the carry in

Csel – a 2-element std\_logic\_vector (00=Cin/01=Cin’/10=’0’/11=’1’)

Func – 4 bit function code (AND = “1000”/OR=”1110”,…)

Addsub – Add or subtract (add=’1’/subtract = ‘0’)

Arlo – Arithmetic or Logic operation (1 = arith/0 = Logic)

OUTPUTS

Result – 8-bit std\_logic\_vector

N – Negative Flag – the msb of the result

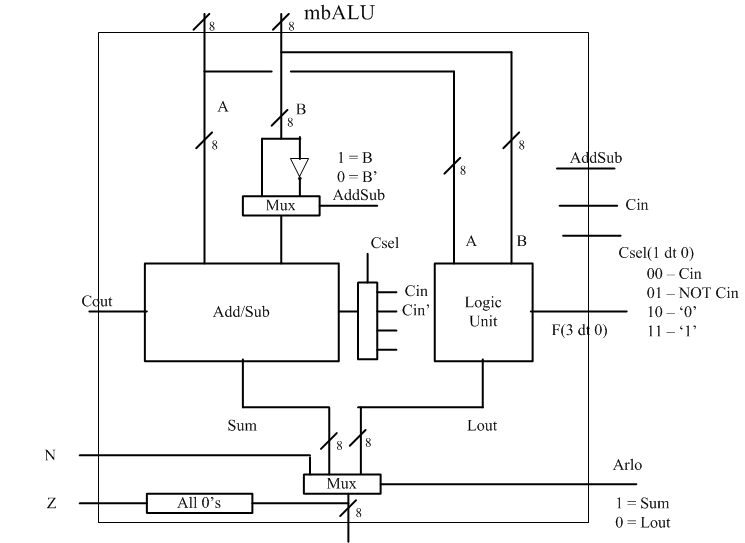
Z – Zero Flag – generated from the nor of all result bits

Cout – the carry out of the adder

Once the entity is done you can declare the components to be used and wire them together.

You will need some local internal signals to connect it all up.

Remember that the ALU has this internal architecture but for the datapath it is just a component:



Create the ENTITY and ARCHITECTURE of the DATA PATH. The TYPE for the signals is std\_logic and std\_logic\_vector. Simulate it in the testbench provided.

Then place the unit and all components in a directory and do the synthesis.

CREATE A REPORT that details all the simulation and synthesis results.