In this assignment you will be implementing the complete ALU microbaby.

Having the various components (all using TYPE std\_logic), it is time to put the ALU of Microbaby together.

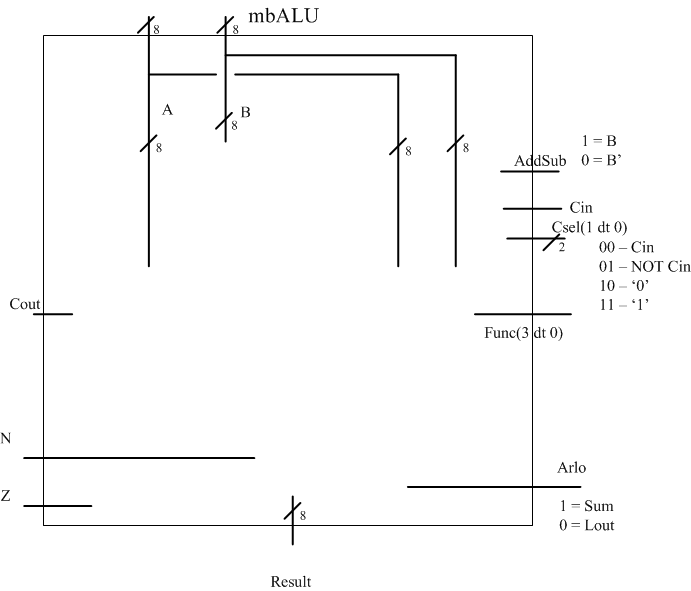
The components at the heart of the ALU are the 8-bit Logic Unit and the 8-bit Adder.

The Logic unit is constructed by using 8 4-to-1 multiplexers. The 4 bit data input of each is connected to the 4 bit Function code. The bits of A and B go the corresponding select inputs. The 8-bit result is generated.



Use the 8-bit carry select adder architecture for the 8-bit adder.

These are enclosed in an interface which is the ENTITY of the ALU.



The signals of the interface:

INPUTS

A,B – 8-bit std\_logic\_vector

Cin – the carry in

Csel – a 2-element std\_logic\_vector (00=Cin/01=Cin’/10=’0’/11=’1’)

Func – 4 bit function code (AND = “1000”/OR=”1110”,…)

Addsub – Add or subtract (add=’1’/subtract = ‘0’)

Arlo – Arithmetic or Logic operation (1 = arith/0 = Logic)

OUTPUTS

Result – 8-bit std\_logic\_vector

N – Negative Flag – the msb of the result

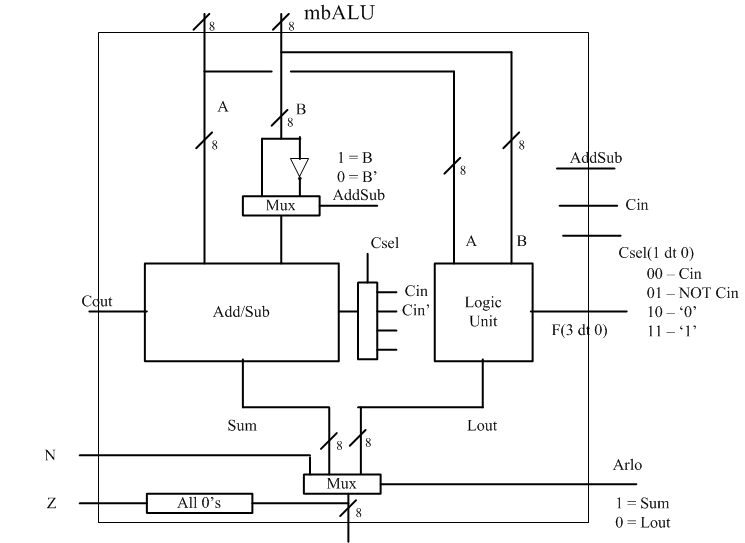
Z – Zero Flag – generated from the nor of all result bits

Cout – the carry out of the adder

Once the entity is done you can declare the components to be used and wire them together.

You will need some local internal signals to connect it all up.

Together it look like:



Once you have your unit completed, use the testbench from the course webpage to simulate the MBALU.

Now completed, take VHDL for all the components used along with the MBALU component and put them in a directory MBALU. You can now run synthesis on the complete MBALU.

CREATE A REPORT that details all the components used and the VHDL of the MBALU.

Also include your synthesis results.