In this assignment you will be exploring the adder for MicroBaby.

The baseline architecture is a simple ripple carry adder.

1. Create a single bit full adder. The interface is shown below.



The function is Sum <= A xor B xor Cin;

 Cout <= (A and B) or (A and Cin) or (B and Cin);

2. Then structurally build an 8-bit adder from this.



3. Create the entity and architecture for a 4-bit 2-to-1 mux.



 R <= (S and A) or (not S and B)

4. Now create a carry select adder with 4 bits in the first stage and 4 bits in the second stage. It is constructed as shown below. Write the VHDL ENTITY and ARCHITECTURE. The ENTITY will have A,B (std\_logic\_vector(7 downto 0)), Cin as inputs and Sum (std\_logic\_vector) and Cout. You will need a few internal signals to connect everything up.



5. Create a VHDL testbench which instantiates both the 8-bit ripple and 8-bit carry select unit. Apply stimulus and compare the results, including the waveform in your report.

6. Synthesize each in Quartis and compare the results. Also use Quartis to find the time from Cin to Cout for each and report that time. Include the details of the synthesis result of each unit in your report.