In this assignment you will be modifying the multiplexors that you created in assignment 1.

Modify the ENITIES and ARHCITECTURES to use TYPE std\_logic and std\_logic\_vector

A 2-to-1 multiplexor

**Write the VHDL ENTITY and ARCHITECTURE for a 2-to-1 multiplexor.**



A 2-to-2 multiplexor by 8 bits

**Write the VHDL ENTITY and ARCHITECTURE for a 2-to-1 multiplexor x 8-bits.**



A 4-to-1 multiplexor

**Write the VHDL ENTITY and ARCHITECTURE for a 4-to-1 multiplexor.**



A 4-to-1 multiplexor by 8 bits

**Write the VHDL ENTITY and ARCHITECTURE for a 4-to-1 multiplexor x 8-bits.**



**The report on this**

Compile the VHDL for the ENTITY, ARCHITURE of the units. Copy all the code into one MS WORD file and submit.