In this assignment you will be creating some of the base components used to structure any processor architecture.

A 2-to-1 multiplexor

**Write the VHDL ENTITY and ARCHITECTURE for a 2-to-1 multiplexor.**



A 2-to-2 multiplexor by 8 bits

**Write the VHDL ENTITY and ARCHITECTURE for a 2-to-1 multiplexor x 8-bits.**



A 4-to-1 multiplexor

**Write the VHDL ENTITY and ARCHITECTURE for a 4-to-1 multiplexor.**



A 4-to-1 multiplexor by 8 bits

**Write the VHDL ENTITY and ARCHITECTURE for a 4-to-1 multiplexor x 8-bits.**



**And Final part of the HDL**

Write a VHDL ENTITY and ARCHITECTURE for a testbench to test each of these. It can be 1 testbench or 4 separate testbenches.

Create a report with the HDL of each of the units (4 separate reports), the testbench and the simulation results.

**QUARTIS synthesis**

Once synthesized, add to the report on each unit the synthesis results.