Homework

Homework 1

Reading:

Textbook Chapter 1 (3rd ed.).

D. Harris webpage: Lecture 0, Lecture 1, and Lecture 2 (all for Chp. 1).

Rabaey et al textbook webpage: Lecture 1

Mircea tutorials: [http://www.ee.virginia.edu/~mrs8n/cadence/Cadencetutorials.html](http://www.ee.virginia.edu/~mrs8n/cadence/Cadencetutorials.html)

**AMI 0.5um Padframe Library, AMI 0.5um Design Library**

Writing:

Chapter 1 Exercises (3rd ed.) 1.4, 1.7, 1.13, 1.14 (only a – c), 1.15 {use OOA instead of not OOA, parts a-c)

6. Compare and contrast the schematics of a D latch vs. a D flip flop with regards to advantages and disadvantages in terms of electrical performance (reliability, speed, power, area, etc.).

7. Approximate the dimensions of the inverter layout in lambda, to the nearest 10 lambda in long dimension, and use half of the long dimension for the short dimension. Use the Layout with 3D Geometry sheet. Using the AMI 0.5um process (use lambda = 0.3um), assume the payload area of a tiny chip is tiled with inverters. Estimate the number of inverters that fit in the payload area.

Homework 2:

Reading Material:

Textbook:
Chp. 1 - 1.6, 1.8-1.12,
Chp. 2 – 2.1, 2.2, 2.5
Chp. 3 - Table 3.1, Fig. 3.8

Webpage:
Beyond Moore’s Law
2nd edition 721 textbook pages
3 pg. doc on bitslice ALU (OM2 chip)
Writing:

1. Draw a stick diagram and schematic for the INVZ, MUX2, and LAT cells in the ami05cell library and explain the circuit strategies. Compare these cells to the versions in the Weste/Harris textbook. Comment on the use of metal2 in a standard cell.

2. Estimate the total length of wire on a 1 sq. cm. Die that uses 4 levels of metal, where the wire is laid out serpentine over the entire die with an 8 lambda pitch (all levels). Use lambda = 0.5um.

3. Discuss why long, high speed digital busses use differential signaling (eg. B and Bbar), and why differential inverter circuits are needed instead of generating Bbar by inputing B into an inverter to yield Bbar.

4. Compare/contrast the slice plan of the bitslice (fig. 1.68 of the textbook) of a datapath with the ALU bitslice description on the class web page from the OM2 Data Path ALU.

Problems from Chapter 2 in the textbook:
2.1 + calculate Reff for each transistor curve.
2.2, 2.14
2.21 (explain your answers)

Homework 3

Study the DC transfer curve of a CMOS inverter, and know the five regions of operation and behavior of the PMOS and NMOS transistors. Work out Problem 2.16

Explain the calculation of the input capacitance of the AMI05 cells in the cell library. Explain the calculation of diffusion capacitance. Both capacitances are described in the SPICE test results for the AMI05 process on the MOSIS web page.

Explain the transient response of CMOS inverters using effective resistance and layout capacitance. Note the relationship between the Reff values of a CMOS gate and the input capacitance the gate presents to the previous stage.
Homework 4

Problems from Chapter 4 in the textbook.

Reading: Review Problem 4.11 for practice.

Writing:

Write a 1 pg description of latchup, and use a metaphor of a latch with MOSFETs to describe the behavior of the parasitic BJT latch in CMOS.

4.10
4.12

Problem using Figure 4.16:
a). Change the final load capacitance from 20 to 72. Calculate $h$ and gate size for each stage. Gate size is how many times larger than minimum.
b). From Part a), show that a design with fewer stages can be faster. Assume the complements of the off-path inputs are available.
c). Change the final load capacitance from 20 to 7200. Calculate $h$ and the gate size for each stage. Discuss how you could speed up the design by adding more stages.