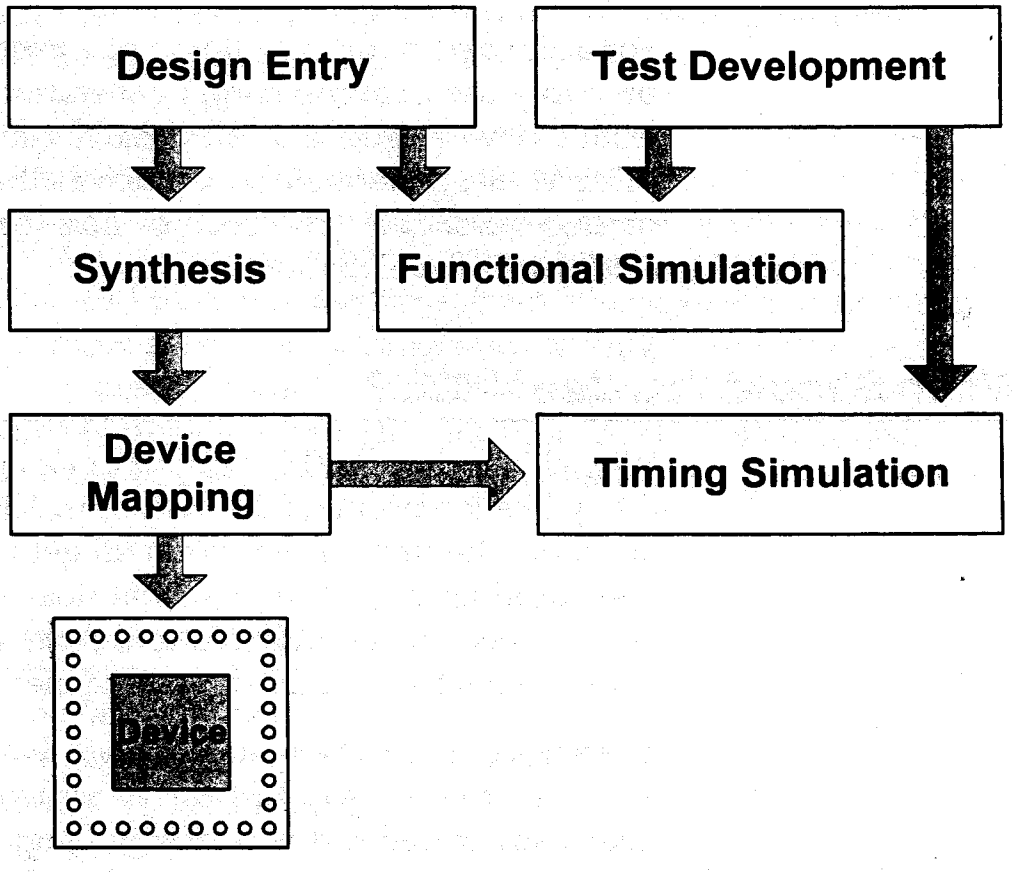
The FPGA/ASIC Design Process

The following diagram shows a simplified design process including both synthesis and simulation, assuming that the target of the process is one or more programmable logic or ASIC chips. The key to understanding this process, and to understanding how best to use VHDL, is to remember the importance of test development. Test development should begin as soon as the general requirements of the system are known.

VHDL can be used for both design and test development.



Where does VHDL fit in this diagram? VHDL (along with other forms of entry, such as schematics and block diagrams), will be used for design entry. After being captured into a